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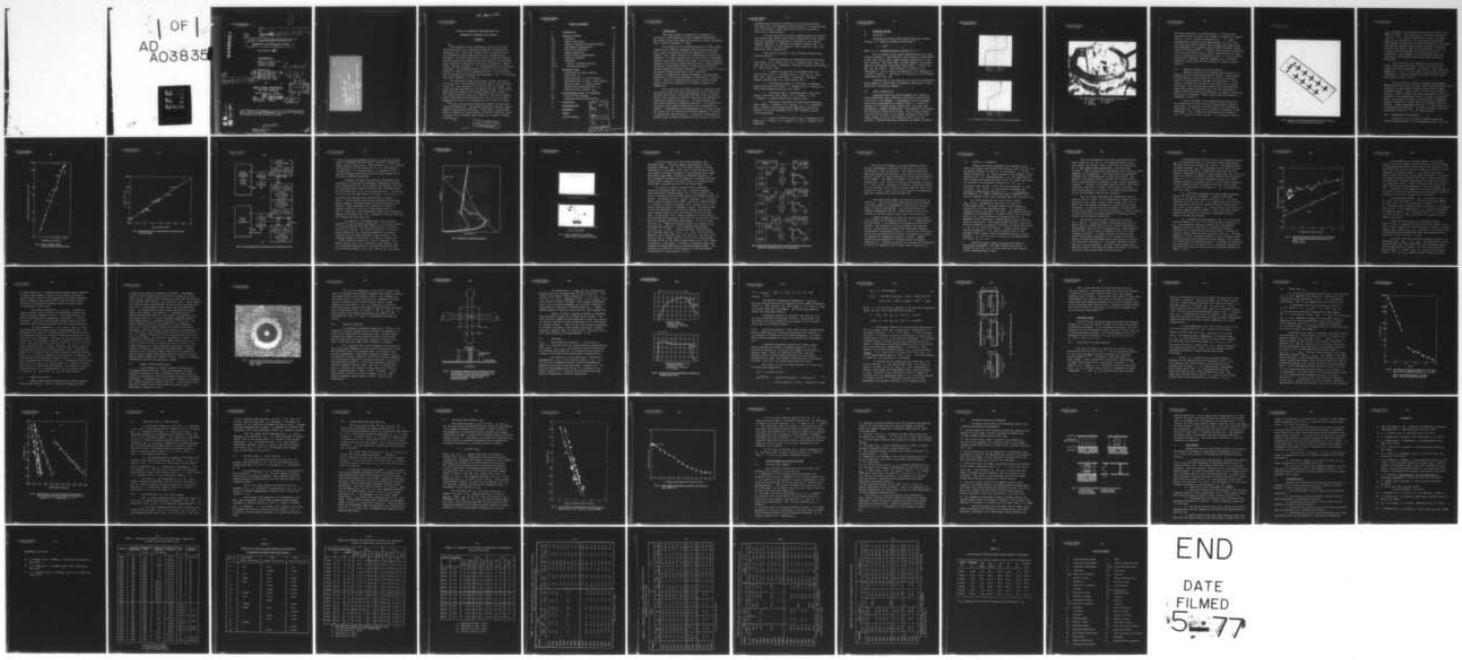

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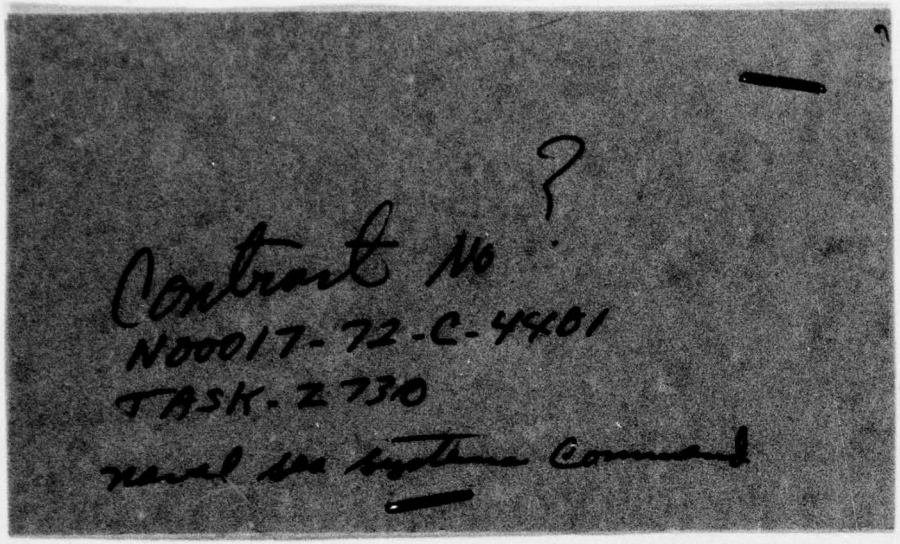
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APL Project Z730

THE JOHNS HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
SILVER SPRING, MARYLAND

A STUDY OF AMORPHOUS SEMICONDUCTORS FOR SYMMETRICAL VARISTOR APPLICATIONS

ABSTRACT

The purpose of the investigation was to study those switching properties of elemental amorphous semiconducting materials (e.g., boron and silicon) which are applicable to electromagnetic pulse (EMP) protection of communications equipment. The major experimental effort during the contract period consisted of measuring switching times and determining their relation to material and electrical parameters. Significant progress was made in: (1) understanding of the switching mechanism; (2) controlling boron resistivity by the introduction of carbon into the amorphous matrix; (3) determining and controlling the switching time parameters, and (4) achieving fast pulse response (< 10 ns).

The transition times include both a delay time and a switching time. The switching time was shown to be controlled by the RC time constant of the device plus the system. The delay time was controlled by the applied voltage. Both single pulse and low frequency oscillating signals were studied. The typical varistor, which was symmetric, had pulse response times (time delay plus switching time) in the 1-10 ns region, capacitance 1-10 pF, and thresholds in the 5-20 volt range.

A model for switching combining thermal and electronic events was formulated. The process depends on voltage, sample geometry and pulsing conditions. A very rapid, high voltage pulse is expected to cause chiefly electronic switching, while a slower rise in voltage signal would lead to mainly thermal switching.

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1. INTRODUCTION

This final report is submitted in reference to APL Project Z730 sponsored by Harry Diamond Laboratories. The report covers investigations carried out during the period July 1, 1972 to December 31, 1974.

The purpose of the investigations was to study those properties of elemental amorphous semiconducting materials (e.g., boron and silicon) which are applicable to electromagnetic pulse (EMP) protection of communications cables and equipment. Of prime interest was the non-linear relationship between current and voltage with either: (a) a rapid transition between a low and high conducting state with unstable negative resistance (switching varistor), or (b)a smooth transition without negative resistance (varistor). In both cases, [a and b], an imposed voltage pulse would cause a manyfold increase in conductivity across the sample, thus providing protection to electronic equipment by shorting the system to ground. The use of amorphous materials may provide rugged devices relatively insensitive to radiation damage and temperature.

Since switching was known to occur in amorphous boron and silicon films, the major experimental effort during the contract period was in measuring switching times and determining their relation to material and electrical parameters. Significant progress was made in: 1) understanding the switching mechanism in amorphous materials; 2) learning how to control boron sample properties by the introduction of carbon; 3) determining those parameters that control switching times, and 4) achieving fast pulse response (< 10 nsec) as required for EMP protection. In addition, switching time studies aided in device modeling and predictions of physical

parameters and constants necessary for practical varistors. The expectation that amorphous boron because of its high melting point and stability could form useful devices is generally borne out by these studies.

A brief review of the entire program along with significant results and future study areas is presented in this report. Detailed background information is contained in the original proposal (APL Ref. No. AD-5334) and Progress Reports Nos. 1, 2, 3 and 4, February 5, 1973, August 5, 1973, April 22, 1974, and August 26, 1974, respectively.

The work has resulted in the following presentations and publications:

1. "Switching Dynamics in Amorphous Boron and Silicon Thin Films", H. K. Charles, Jr. and C. Feldman, Amer. Phys. Soc. Bull. 19, 361 (1974). Presented: APS March Meeting, Philadelphia, Pa., March 24-28, 1974.

2. "A Model for Switching in Amorphous Boron and Silicon Thin Films", C. Feldman and H. K. Charles, Jr., Amer. Phys. Soc., Bull. 19, 362 (1974). Presented: APS March Meeting, Philadelphia, Pa., March 24-28, 1974.

3. "Electrothermal Model of Switching in Amorphous Boron and Silicon Thin Films", C. Feldman and H. K. Charles, Jr., Solid State Communications 15, 551 (1974).

4. "Switching Times in Amorphous Boron, Boron Plus Carbon, and Silicon Thin Films", H. K. Charles, Jr. and C. Feldman, J. Applied Physics 46, February 1975.

5. "Electrical Properties of Carbon-Doped Amorphous Boron Films", C. Feldman, H. K. Charles, Jr., F. G. Satkiewicz and J. Bohandy, Fifth International Symposium on Boron and Borides, to be held September 8-11, 1975, Bordeaux, France (to be published).

6. A paper on switching delay times in amorphous boron films by G. W. Turner, H. K. Charles, Jr. and C. Feldman (to be submitted).

2. TECHNICAL REVIEW

2.1 Varistors

Varistors are devices which show non-linear current-voltage (I-V) behavior, generally described by

$$I = K_o V^n$$

where K_o is a phenomenological constant and $n > 1$.

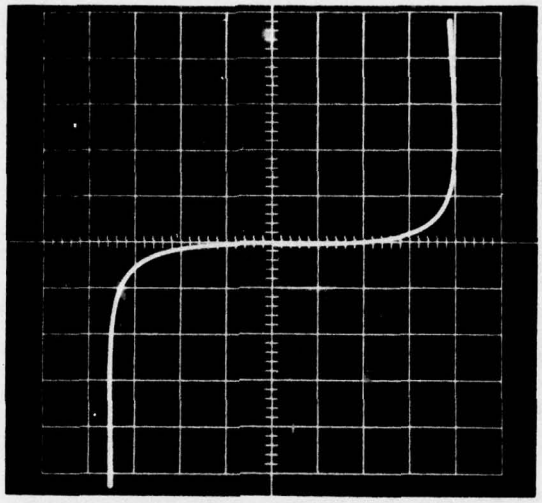
The two types of non-linear characteristics are illustrated in Figure 1. Both exhibit a low (non-zero) conductivity in the "OFF" state, and a large (finite) conductivity in the "ON" condition. One type (Fig. 1B) also exhibits an unstable negative differential resistance (NDR) region [1] between the OFF and ON states. This behavior is referred to as "switching" [2] and is usually accompanied by the formation of a current filament [3]. Hysteresis is observed in the switching characteristics (Fig. 1B).

Although NDR is not necessary for varistor applications, prime emphasis in this study was placed on switching in amorphous boron and silicon samples.

2.2 Sample Fabrication

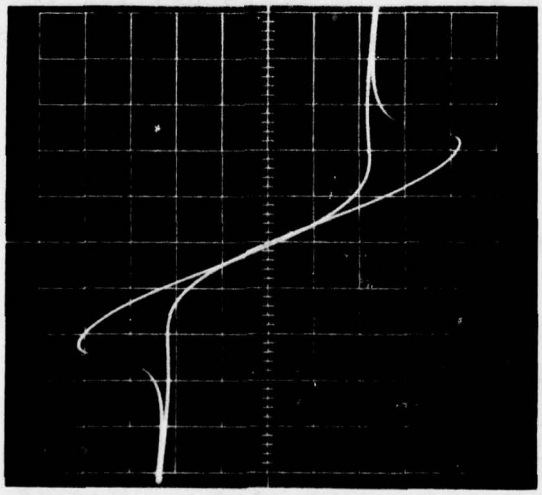
Amorphous boron and silicon samples were formed by vacuum deposition under conditions which were varied during the course of the program. A photograph of the arrangement within the vacuum chamber is shown in Fig. 2. As much as possible all fittings, wires, screws, etc., are made from molybdenum to reduce contamination. The windows in the shutter are fitted with fused silica slides. One of these windows lines up with the hole in the heater allowing a clear view from a window on top of the stainless steel jar to the crucible. Typical deposition conditions are given in Table I.

(A)



SAMPLE	Si49
VERTICAL	0.5mA/DIV
HORIZONTAL	2V/DIV

(B)



SAMPLE	B89A
VERTICAL	2mA/DIV
HORIZONTAL	2V/DIV

Fig. 1 VARISTOR CHARACTERISTICS (A) NON-SWITCHING (B) SWITCHING

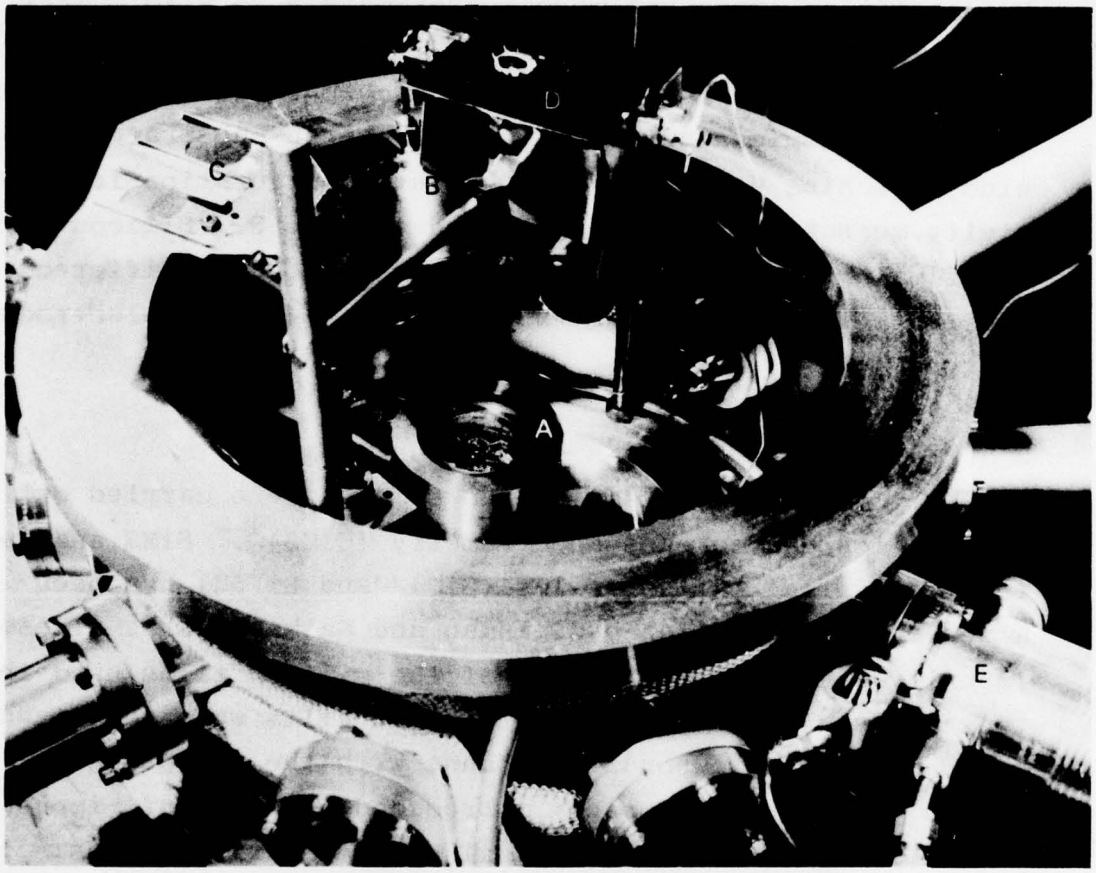


Fig. 2 Electron Gun and Crucible Arrangement m Vacuum System

A) Crucible B) Electron Gun
C) Shutter D) Heaters
E) Leak Value

The source material, of highest purity, in water-cooled, molybdenum-lined crucibles, was brought to deposition temperature by 15 keV electron bombardment at 1 to 2 kW. Predeposition pressures were approximately 5×10^{-9} Torr. The films were placed between two titanium electrodes which were deposited in a separate vacuum chamber to avoid contaminating the semiconductor. A typical boron substrate containing nine switching devices and a 4-point configuration for resistivity measurements is illustrated in Fig. 3. Silicon devices had similar electrode crossover geometry, but a different substrate layout which did not include a 4-point electrode pattern.

2.3 Impurity Analysis and Carbon Doping

Impurity analyses of the samples were carried out by sputter-ion source mass spectrometry (SIMS)[4]. SIMS analysis for two typical silicon films (Si 42 and Si 52) has been given in a publication by Feldman and Satkiewicz [4]. These impurity contents are typical of the silicon films used in this study. For the most part, boron films were deposited under more uniform conditions and, with the exception of carbon which was purposely introduced as a dopant, impurities were held to a minimum. Typical boron impurity analysis is presented in Table II.

Carbon was added to the samples during deposition by introducing acetylene into the vacuum chamber through a leak valve. The control of carbon content was achieved by monitoring the C^{12} peak with a residual gas analyzer during deposition. Fig. 4 shows the experimental data relating the C^{12} peak and carbon content. It is believed that the

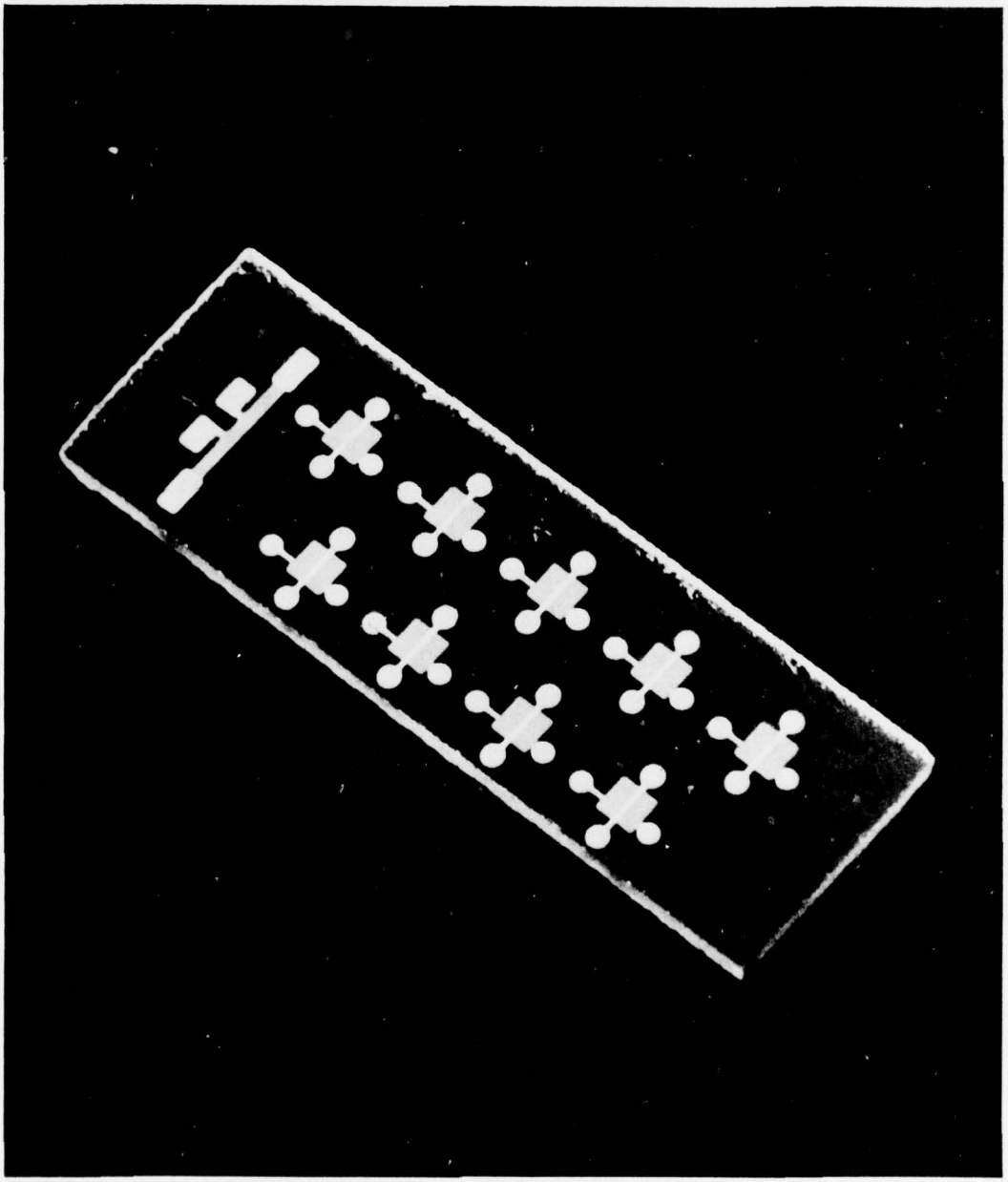


Fig. 3 Amorphous Thin Film Switching Sample: Illustrating 9 Switching Devices and 1 Four-Point Resistance Configuration

C_2H_2 decomposes at the molten boron surface producing the required carbon. The fused silica substrates were maintained at $300^{\circ}C$ during deposition in order to minimize C_2H_2 or H_2 absorption. The sputter-ion source mass spectrometer was also used to check the purity of the samples. The hydrogen content was monitored and found to increase slightly with higher C_2H_2 partial pressure. It is not believed that the hydrogen affected the electrical properties. Early samples containing carbon which was introduced from a graphite boat also showed increased resistance.

The major effect of carbon was to increase the sample resistivity and, hence, produce varistors with higher OFF state resistances. In addition, high resistance samples (i.e., $R > 1.5$ to $2.0K\Omega$) always switched at room temperature. A plot of sample resistivity versus carbon percentage is given in Fig. 5.

The resistivity initially increases approximately exponentially with carbon content (linear semilogarithmic plot), suggesting a compensation mechanism rather than a simple trapping behavior. Above 14% C the resistivity tends to saturate. Recent efforts have been concerned with the understanding of the compensatory effect of carbon in amorphous boron. Sensitivity to impurity concentration in amorphous materials appears to be less than in crystalline semiconductors. Carbon percentages less than 1% had little effect on amorphous film behavior. The range of carbon impurities considered to date is 1 to 16 atomic percent.

2.4 Measurement Configuration

Switching times and current voltage curves were observed simultaneously by the arrangement shown in Fig. 6A.

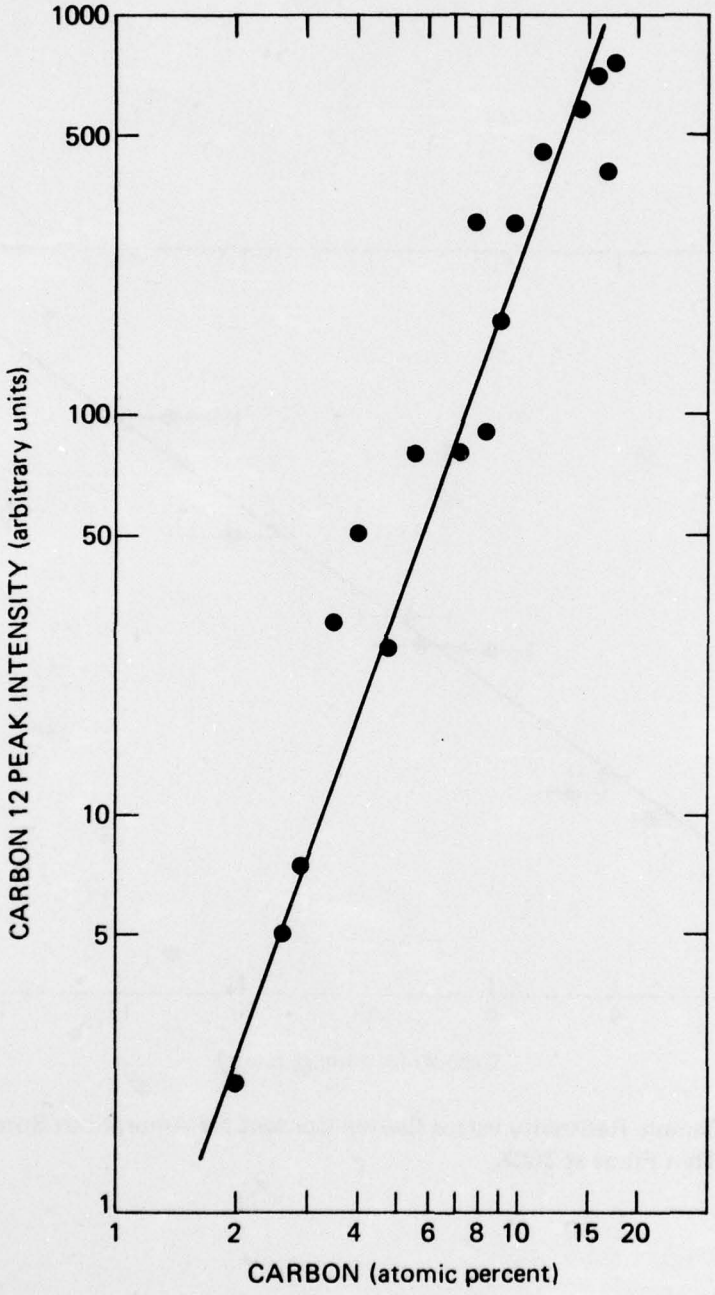


Fig. 4 Intensity of Carbon 12 Peak versus Amorphous Film Carbon Content

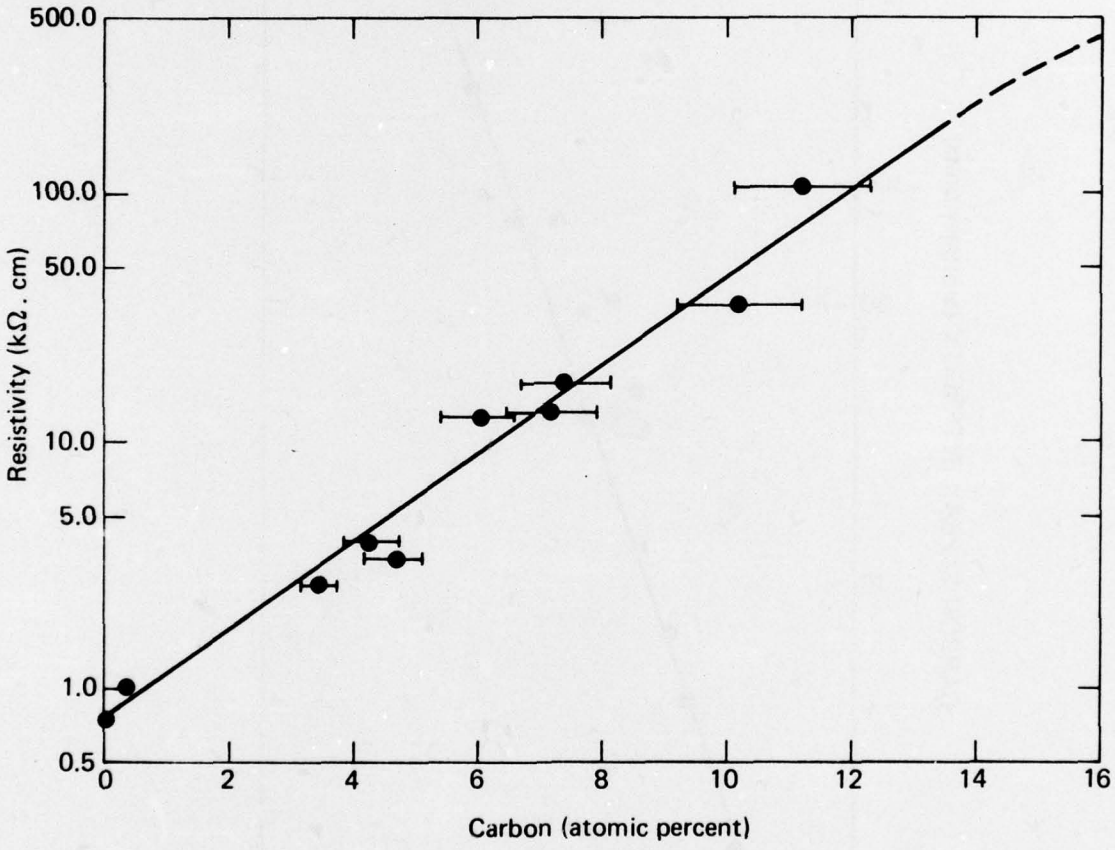


Fig. 5 Sample Resistivity versus Carbon Content for Amorphous Boron Thin Films at 300K

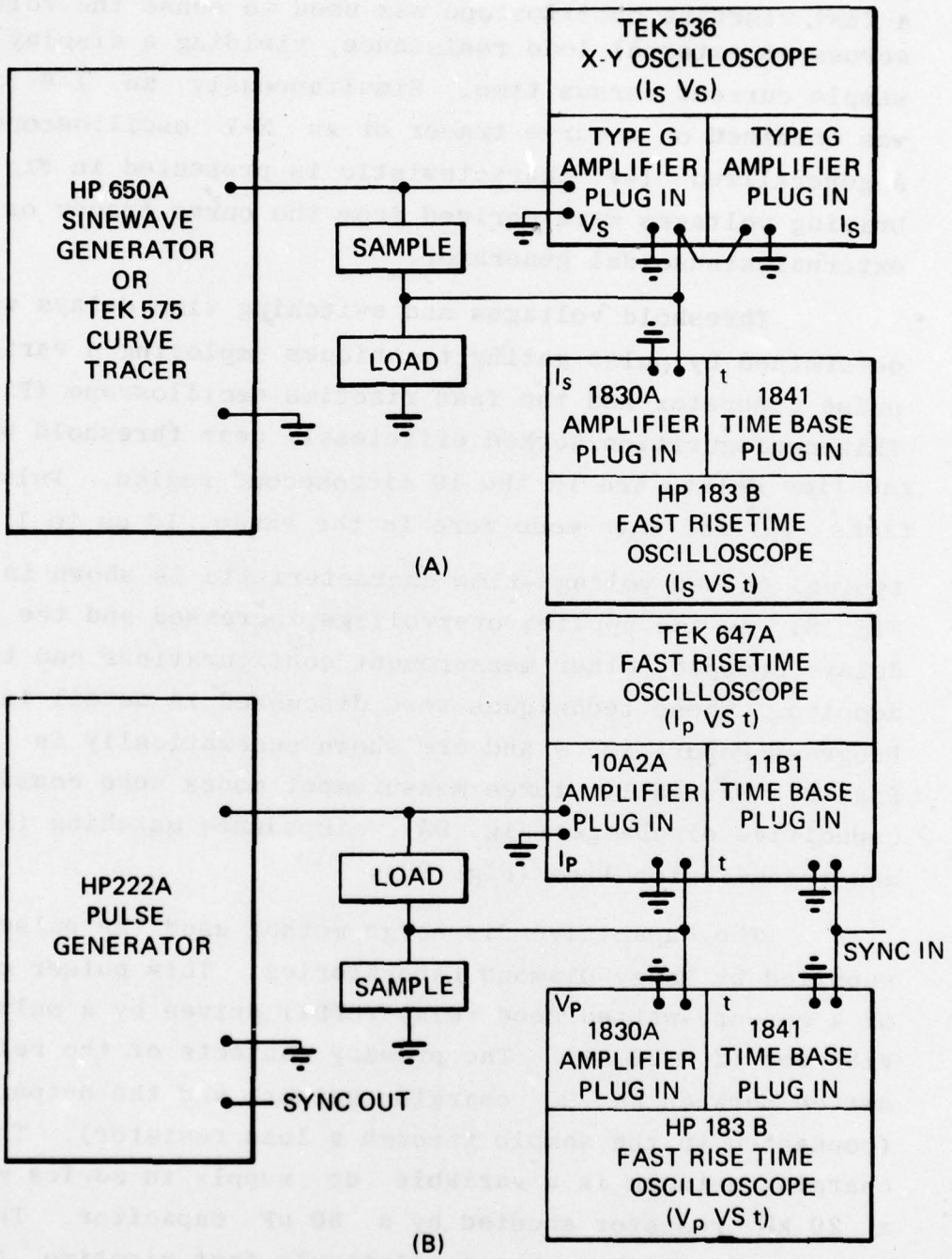


Fig. 6 Block Diagram Measurement Configurations (a) Steady State (b) Pulse

A fast risetime oscilloscope was used to sense the voltage across an external load resistance, yielding a display of sample current versus time. Simultaneously, an I-V display was obtained on a curve tracer or an X-Y oscilloscope. A generalized I-V characteristic is presented in Fig. 7. Driving voltages were derived from the curve tracer or an external sinusoidal generator.

Threshold voltages and switching time delays were determined by pulse gating techniques employing a variable pulse generator and the fast risetime oscilloscope (Fig. 6B). This configuration worked efficiently near threshold where the time delays are in the 10 microsecond region. Pulse durations (T_D) for this mode were in the range 10 μs to 1 ms. A typical pulsed voltage-time characteristic is shown in Fig. 8. As the applied overvoltage increased and the time delays dropped, other measurement configurations had to be adopted. These techniques were discussed in detail in Progress Report No. 4 and are shown schematically in Fig. 9. Basically, three measurement modes were considered: capacitive discharge (Fig. 9A), impedance matching (Fig. 9B), and transmission line (Fig. 9C).

The capacitive discharge method used the pulser supplied by Harry Diamond Laboratories. This pulser consists of a mercury-wetted reed relay (SPDT) driven by a multivibrator ($f \simeq 20$ Hz). The primary contacts of the relay switch between an RC charging network and the output (connected to the sample through a load resistor). The charging network is a variable dc supply in series with a 20 kΩ resistor shunted by a 80 μF capacitor. The output voltage (V_p) has a relatively fast risetime (T_R) with adjustable amplitude and a period determined by the multivibrator frequency (e.g., T_R = 100 ns, V_p = 10 volts).

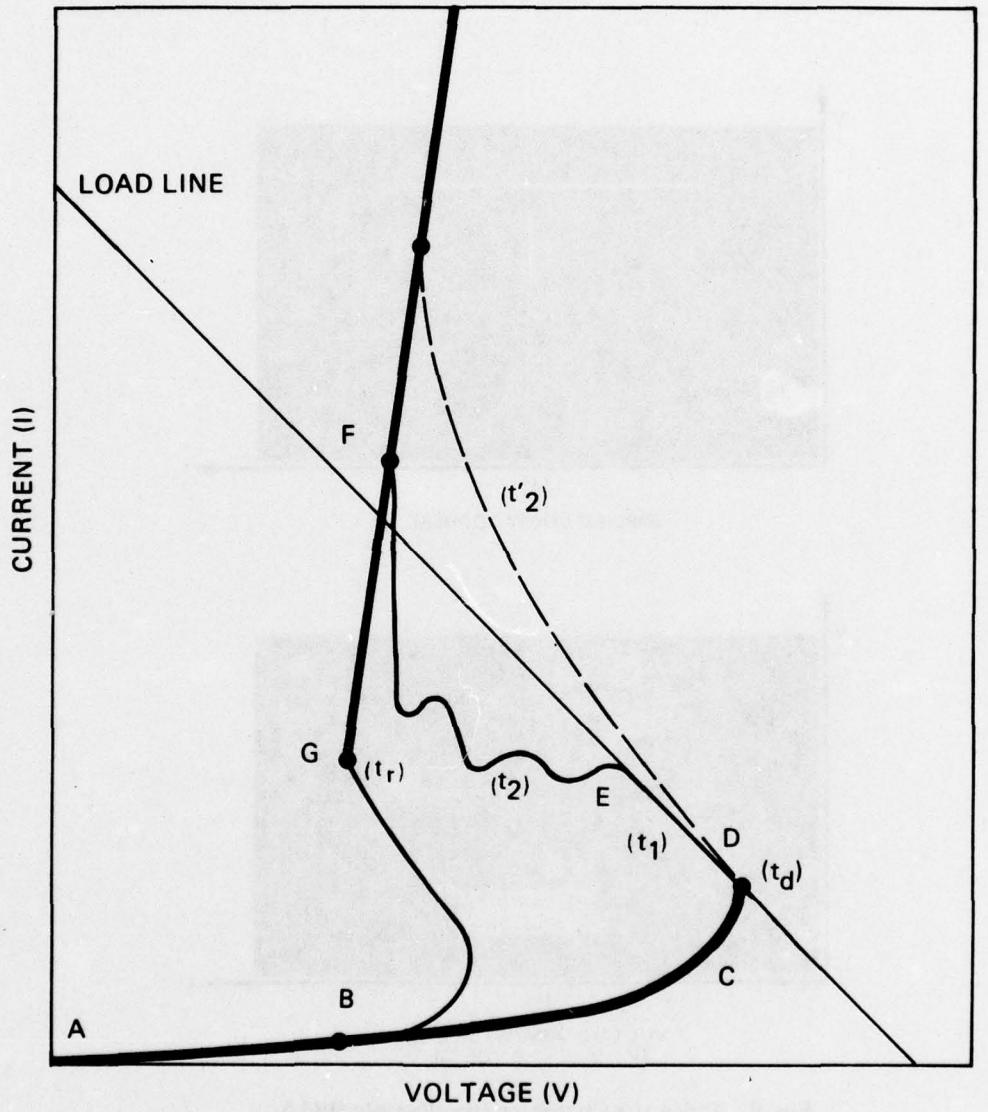
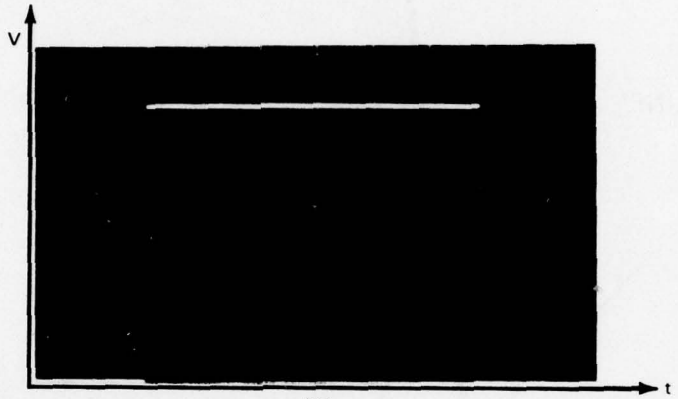
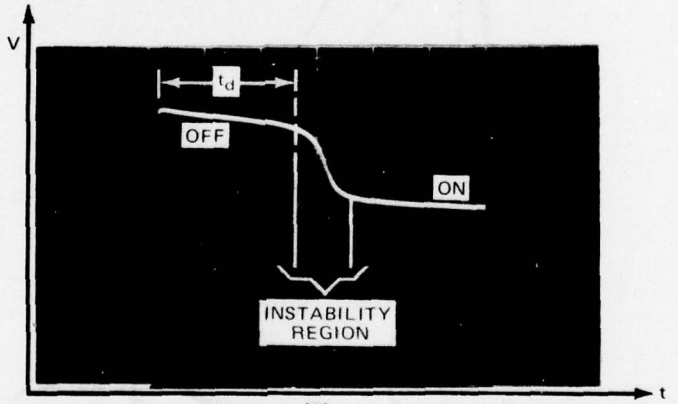


Fig. 7 Generalized I-V Switching Characteristic



(A)

APPLIED VOLTAGE PULSE



(B)

VOLTAGE ACROSS SAMPLE
($V = V_{TH} + 1.0$ VOLTS)

Fig. 8 Pulse V-t Characteristics Sample B81A (Vertical: 2V/Div Horizontal: 1.5 μsec/Div)

For delay times less than one microsecond, two problems arose: (1) pulse ringing (oscillations) due to impedance mismatch, and (2) an excessive amount of energy dissipation in the sample (duty cycle 0.15) because of the high applied voltages necessary to reach shorter delay times. Microprobe capacitance limitations (Progress Report No. 4) were eliminated by mounting the sample in a shielded box with coaxial (BNC) connectors and short leads (to minimize stray capacitance) soldered directly to the sample pads.

To solve the ringing inherent in the unmatched capacitive discharge mode (Fig. 9A), a passive impedance matching network (Progress Report No. 4) was designed to be used in conjunction with the HDL pulser or a Tektronix Model 110 pulser. The Model 110 has a 0.25 ns risetime (V_p = 50 volts) using a mercury-wetted relay (SPDT), driven by a multivibrator ($f \simeq 700$ Hz), to switch a charged 50 Ω coaxial line to the output and then back to a charging circuit. The output pulse is half the amplitude of the initial charged line voltage with a period equal to twice the transit time of the delay line. To match the 50 Ω output impedance of the pulser to the high OFF state impedance (typically 2 k Ω) of the switching device, a minimal loss L-pad was designed. An active probe (HP 1120, $Z_{in} \simeq 1M\Omega$) was connected across the sample and the switching was observed on a fast risetime oscilloscope (HP 183B, $T_R < 1.5$ ns). This system (Fig. 9B) provides a fast risetime pulse ($T_R \simeq 20$ ns, V_p = 15 v) with variable amplitude and pulse width ($T_D \sim 80 - 500$ ns). The duty cycle (with a 125 ns delay line) is 0.175×10^{-5}, which allows the application of very high voltage pulses with little energy dissipation in the sample. Problems in achieving large overvoltages are encountered due to matching network losses. The network also limits the total risetime of this measurement configuration to approximately 35 ns.

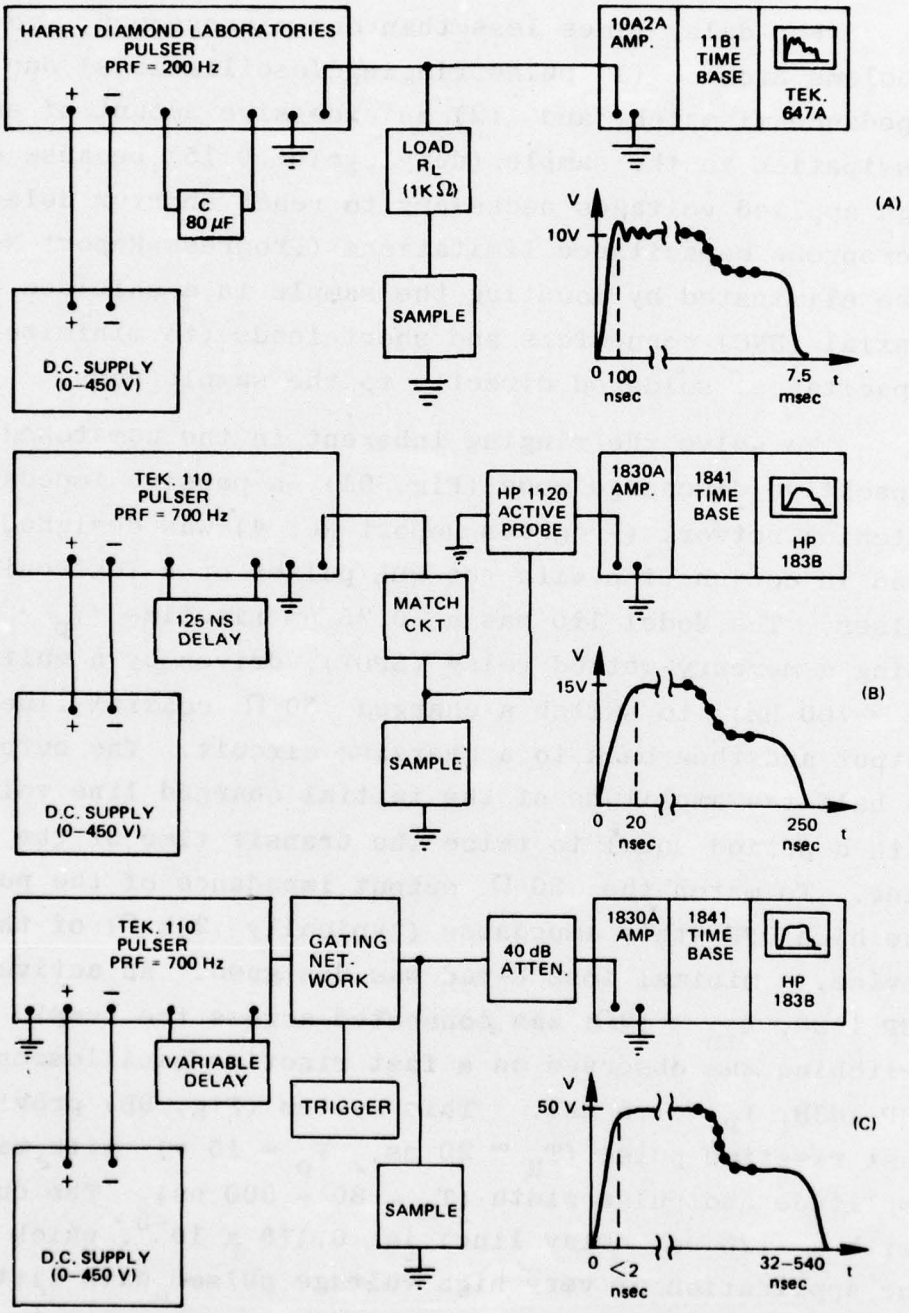


Fig. 9 Measurement Block Diagrams with Typical Pulse Waveforms (a) Capacitive Discharge (b) Impedance Matching (c) Transmission Line

To achieve risetimes in the one nanosecond region at high overvoltages (typically 50-100 volts), the system illustrated in Fig. 9C was used. This system employs the same pulse generation system as in Fig. 9B, but the output is gated to achieve a single pulse which is then applied directly to the sample. The sample is placed in shunt with a 50 Ω transmission line. The fast risetime oscilloscope, buffered by a 40 dB (50 Ω) attenuator, is used to observe the change in line impedance as the device switches from the high to low resistance state. Delay times on the order of one nanosecond have been measured with this configuration.

The delay times possess an inherent statistical uncertainty [5] and all the delay times quoted are the average of a large number of measurements (typically 30) for each value of applied overvoltage. All switching times are averages determined from the 10-90% points of the rising current or falling voltage versus time characteristics.

Sample resistances in both the low and high conductivity states were determined from the I-V characteristics. The resistance of the deposited electrodes was taken into account. The resistivity for boron samples was measured by the 4-point probe technique using deposited titanium electrodes as illustrated in Fig. 3. For silicon, the resistivity was calculated from the device resistance (low field) by applying the appropriate geometric factors. Sample capacitance was measured by standard bridge techniques (Section 2.6). Filament existence and location were determined by the use of applied liquid crystal layers (Section 2.7).

2.5 Electrical Parameters

Typical electrical parameters for amorphous boron, boron plus carbon, and silicon thin films at both 300 and 77 K are given in Tables III and IV. In the tables, ρ_s is the sample resistivity, R_s the resistance at low voltage (linear portion of the I-V characteristic), C_s the capacitance at high voltage (non-linear portion of the I-V curve just prior to switching) as discussed in Section 2.6, and τ_{RC} a calculated time constant. Note that the resistance R used to compute τ_{RC} is not R_s, but rather a discharge path resistance as described in Section 3.7. C corresponds to the measured C_s times a correction factor necessary to reduce all samples to the same cross-sectional area (Section 2.6).

R_s after switching (dc, curve tracer, pulser ($T_D \geq 10\ \mu s$)) decreased by less than 3% from its before-switch value. The major portion of the change occurred after the first switching event. R_s appeared to stabilize after a few events (10 - 100) and remained constant regardless of testing mode. In boron devices, the calculated value of ρ_s after switching was compared with the ρ_s measured by the independent 4-probe method (where switching does not take place). The values agreed favorably within the limits of geometric tolerances (including the small corrections, 1 - 3%, in R_s due to switching). 4-point resistivities were not measured at 77 K due to instabilities in the extremely small current values necessitated by the 4-point geometry. ρ_s at 77 K may, of course, be determined from the device R_s at 77 K.

Switching events caused no observable change in low voltage capacitance. The high voltage capacitance, C_s, changed by less than 2% in going from pre-cycled values to post-switching event values.

The close agreement of the pre- and post-switching event values of R_s and C_s for amorphous boron, boron plus carbon, and silicon films, as well as the equivalence of 2- and 4-point probe measurements, indicated that forming [6] under the described experimental conditions ($T_D \geq 10\,\mu s$) appeared to be negligible. The temperature-time parameters necessary for crystallization in boron and silicon[7] are probably sufficiently large to prevent any forming effects due to crystallization as observed in more complex amorphous systems [6]. Because of the short duration of the EMP pulse (typically less than 0.1 ms[8]) and the lack of forming, these films appear to be suited to the EMP-Varistor problem as far as recoverable devices are concerned.

The ON state resistance was determined from the slope of the ON state I-V characteristic (Region F, Fig. 7). Using the curve tracer, typical values ranged from 100 to 300 Ω with the primary contribution coming from electrode resistance. Correcting for the electrodes, filament resistances on the order of 10 Ω were determined. Slight increases in this resistance value were noted with increasing carbon content and decreasing temperature.

Preliminary results under single pulse testing ($T_D \leq 500$ ns) indicate filament resistances the order of 100 Ω, which is higher than the curve tracer measurements. This suggests that heat due to processes with time durations greater than 10 μs plays an important role in the final filament resistance. A higher filament resistance under short single pulse conditions is to be expected from the theory of switching developed during the course of the work and described in Section 4.2. The exact resistance values have not yet been explored. The most recent samples were made with thicker electrodes to reduce the overall ON state resistance and provide better varistor action.

As described above (Section 2.4), the threshold voltage V_{th} was determined from dc and curve tracer measurements. For pulse durations greater than 10μ sec the apparent pulse threshold voltage, V_{th}', was independent of the pulse duration and consistent with V_{th}. Recent work indicates that the apparent threshold for short duration pulses (for $T_D < 500$ n sec) tends to increase as reported by Shaw, Holmberg, and Kostylev [6]. Values of V_{th} in the pulse independent region for typical samples are given in Tables V and VI. Virgin devices appeared to have slightly higher thresholds (~3%) than curve tracer cycled units with most of the change in V_{th} occurring after the first switch.

V_{th} had little dependence on major sample parameters except for OFF state resistance. A plot of threshold voltage versus OFF state sample resistance (R_s) for boron samples is given in Fig. 10. V_{th} appeared to be an increasing exponential function of sample resistance which implies that, for a given geometry, V_{th} would increase with resistivity and hence sample impurity content. Thus, controlled carbon doping could tailor the threshold of amorphous varistor devices for EMP applications.

V_{th} increased by approximately 25% as the temperature was lowered to 77 K. No direct thickness dependence of V_{th} was observable implying, possibly, that the geometric thickness has to be replaced by an effective thickness (Section 4.2) in modeling of switching events. Silicon displayed a similar trend with more scatter (Table VI). Silicon samples of a given resistance seemed to have a slightly higher threshold voltage than equivalent boron samples. This result is inconsistent with previous studies [9], although the comparison was never made on a resistance basis. Threshold voltages for both boron and silicon increased with decreasing temperatures (300 K - 77 K).

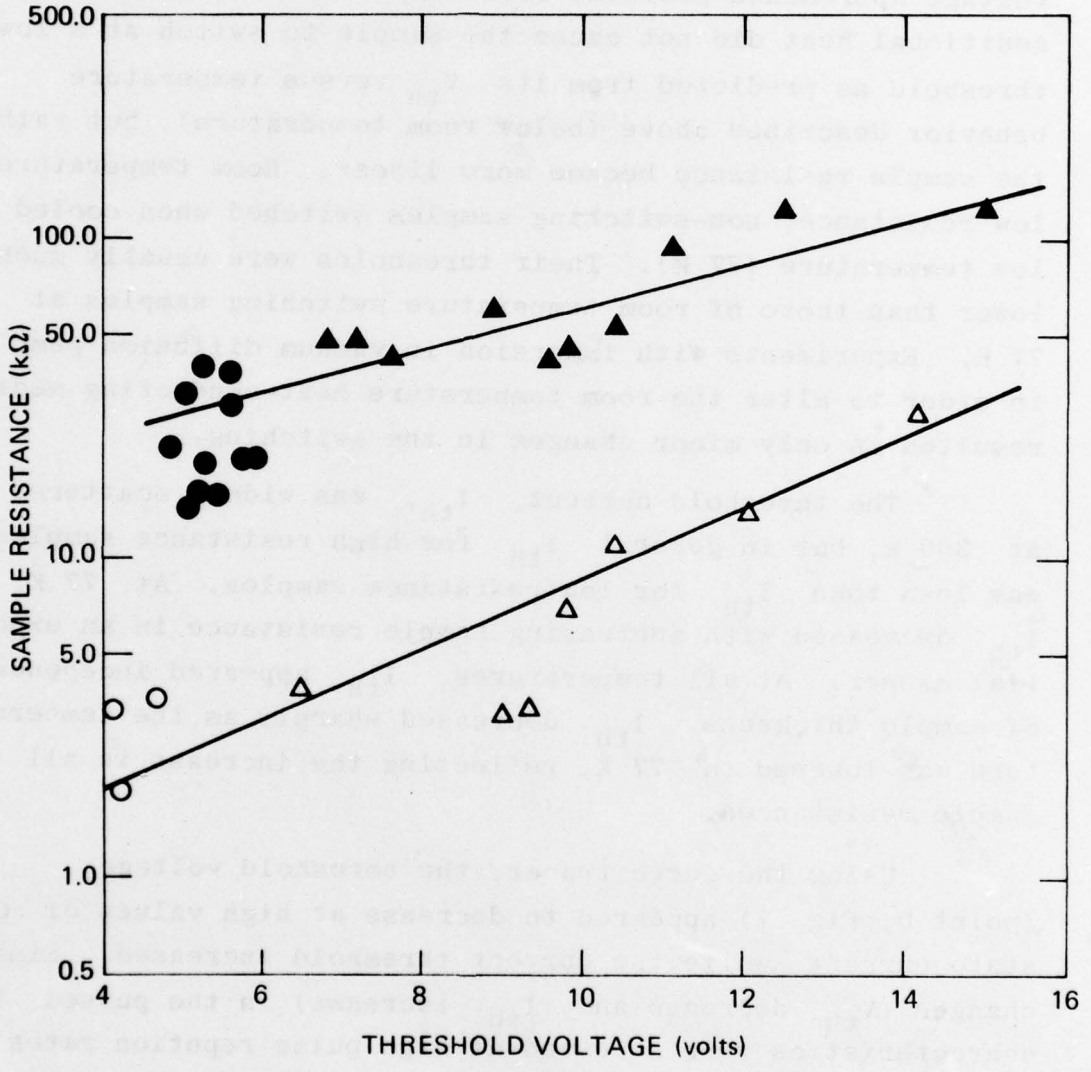


Fig. 10 Threshold Voltage versus Sample Resistance (Low Voltage) Amorphous Boron and Boron Plus Carbon Thin Films.
300 k; ○ , B+C △
77 k; ● , B+C ▲

Room temperature switching samples, when rapidly heated by electric blower, failed to switch even when sample voltage approached previous room temperature threshold. The additional heat did not cause the sample to switch at a lower threshold as predicted from its V_{th} versus temperature behavior described above (below room temperature), but rather the sample resistance became more linear. Room temperature, low resistance, non-switching samples switched when cooled to low temperature (77 K). Their thresholds were usually much lower than those of room temperature switching samples at 77 K. Experiments with immersion in vacuum diffusion pump oil in order to alter the room temperature heat-conducting medium resulted in only minor changes in the switching.

The threshold current, I_{th}, was widely scattered at 300 K, but in general I_{th} for high resistance samples was less than I_{th} for low resistance samples. At 77 K, I_{th} decreased with increasing sample resistance in an exponential manner. At all temperatures, I_{th} appeared independent of sample thickness. I_{th} decreased sharply as the temperature was lowered to 77 K, reflecting the increase in all sample resistances.

Using the curve tracer, the threshold voltage (point D, Fig. 7) appeared to decrease at high values of ON state current, while the current threshold increased. Similar changes (V'_{th} decrease and I_{th} increase) in the pulsed I-V characteristics were observed at high pulse repetion rates (typically 1 kHz with $T_D \simeq 0.1$ ms).

As can be seen from the data in Tables V and VI, the threshold power, P_{th} ($= V_{th} \times I_{th}$), was independent of both thickness and OFF state resistance, but decreased sharply as the temperature was lowered. At high pulse repetition rates or high ac steady state ON current values (curve tracer), the $V_{th} \times I_{th}$ product showed a slight increase.

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At room temperature, a carbon-containing boron sample appeared to require more power to switch than a similar resistance silicon sample, while at low temperature, the high resistance silicon required more power than the high resistance boron. Equivalent low resistance samples seemed to require about the same power in each case.

The holding quantities, V_h, I_h, P_h, displayed a slight increase (large scatter) with thickness and with OFF state resistance (Tables V and VI). The holding voltage increased with decreasing temperature, while both I_h and P_h decreased. High ON state currents (curve tracer) and high repetition rate pulsing tended to raise all holding quantities.

Recovery parameters, V_r, I_r, and P_r (Point G, Fig. 7) were determined from curve tracer (dc) measurements only. The nanosecond fall times of the pulses used in the single pulse and low repetition pulse testing modes prevented observation of this relatively slow phenomenon. Although the time dynamics of device turnoff was not explored in detail, it appears to be very rapid (i.e., consistent with the pulse fall time for $T_D < 0.1$ ms and pulse repetition rates < 1 kHz), indicating that little heating has taken place during pulse applications. Thus, these devices appear to be ideally suited for rapid recovery under EMP environments. V_r, I_r, and P_r appeared to increase with increasing thickness and OFF state resistance (Tables V and VI). V_r increased with the temperature decrease, while I_r decreased during the drop from 300 K to 77 K. The return power P_r seemed to increase slightly as the temperature was lowered. The passage of high ON state currents (i.e., long duration in the ON state) tended to increase V_r, while both I_r and P_r were reduced.

2.6 Sample Capacitance

Sample capacitance was measured on a bridge (General Radio, Model 1656) at 1 kHz at both low voltages and high

voltages with peaks near switching threshold. The measured values at high voltage levels are given in Tables III and IV. These values, corrected for uniform area, were used to calculate the switching time constant τ_{RC} discussed later. Boron samples with numbers higher than B88 had the same cross-sectional area. Similarly, silicon samples above Si49 also had consistent areas. The capacitance at high voltage was generally larger than at low voltage. The value of C decreased as the applied voltage was reduced to low levels, and approached the calculated value of C from the measured geometric factors and assumed physical constants (typically 1 to 10 pF). The higher capacitance may be attributed to a hot conducting region in the center which reduced the effective capacitor thickness. This hot region will be discussed later (Section 4.2). The capacitance, under single pulse condition as illustrated in Fig. 9C, appears to approach the low voltage geometrical value. For a given sample, the capacitance decreased by 10-20% as the temperature was lowered to 77 K. Sample capacitance for a given electrode area and thickness decreased slightly as the carbon percentage in boron increased, suggesting a possible change in dielectric constant with carbon content. Further evidence of this possible change comes from film appearance: pure or lightly doped films appear metallic and gray in color; heavily doped samples are reddish in color. Index of refraction experiments have not been performed to date.

2.7 Liquid Crystal Observations

In all samples a current filament was observed to be present during switching. This was determined at room temperature through the use of liquid crystal layers used to observe the temperature rise on the sample surface as described previously. A photomicrograph of a typical filament as observed with liquid crystals is shown in Fig. 11. In the liquid nitrogen bath, a small bubble formed above the active region, indicating a temperature rise.

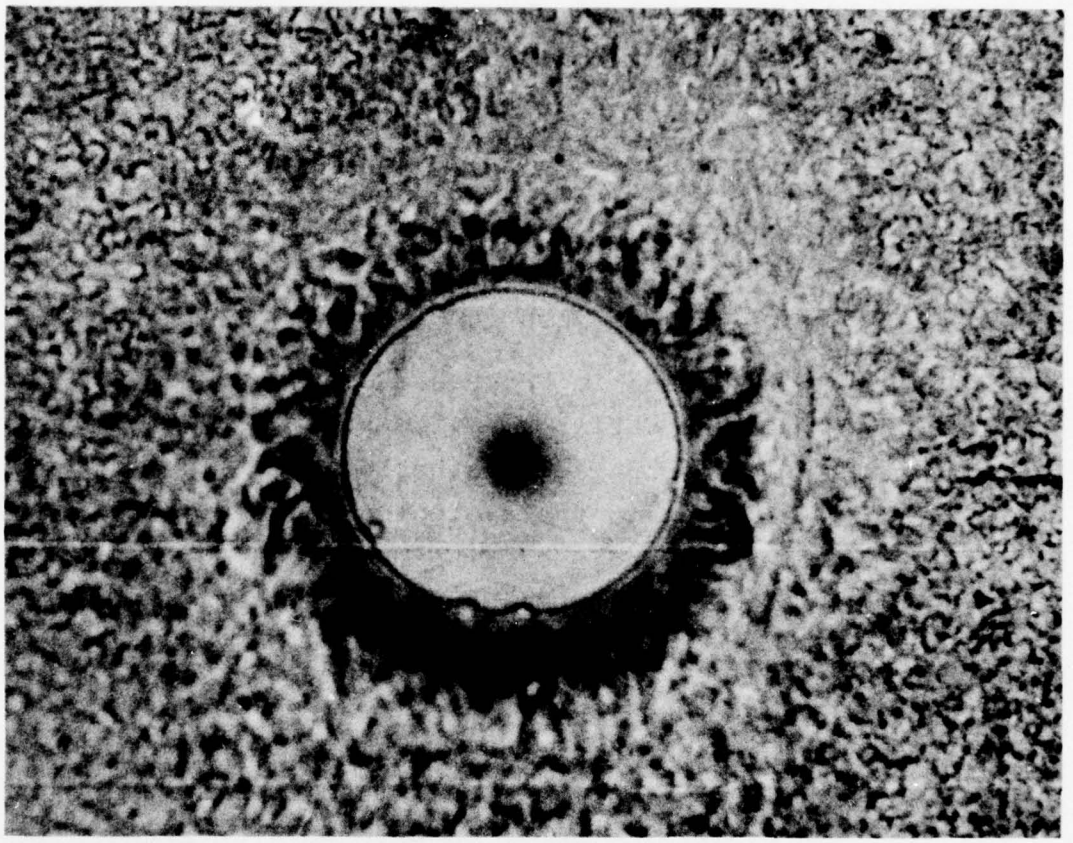


Fig. 11 Pattern Formed, After Switching, in Cholesterol Ester (Liquid Crystal) Spread Over Surface of Amorphous Boron Device (Magn. ~ 240 X)

The size and appearance of the liquid crystal areas above the filament were carefully examined and related to switching characteristics and filament current. The filaments for the steady state t_2' modes (Section 3.4) appeared to be much larger in diameter (for a given current) and at a lower temperature than those of $t_1 - t_2$ (Sections 3.3 and 3.4). They were always located at the edge of the effective electrode area as indicated in Fig. 12, Point 2. The t_p and $t_1 - t_2$ mode filaments were always located near the center of the electrode area (Fig. 12, Point 1) and appeared narrower and hotter.

2.8 Frequency Response

As discussed in Progress Reports Nos. 1 and 2, it is imperative that the varistor device present high impedance (if used in the common parallel protection mode - coaxial center conductor to ground) to the protected units at their upper dynamic range limit and operating frequency, typically less than 0.233 volts rms (Odbm, 50 Ω system) at 100 MHz.

It is apparent that if the equipment to be protected has a high input impedance it will be less sensitive to a given EMP amplitude than a low impedance unit, thus reducing the varistor requirement. High input impedance, however, forces the parallel varistor element to have an even greater impedance at the operating frequency to prevent undue loss. For a given amplitude input signal, a 1 MΩ input impedance requires a varistor impedance greater than 3.86 MΩ to produce less than a 1 decibel (db) change in input power level, while a 50 Ω system requires at least a 193 Ω varistor. If the requirements are held to a more stringent 0.1 db, then varistor impedance levels jump to 50 MΩ and 2.5 kΩ, respectively.

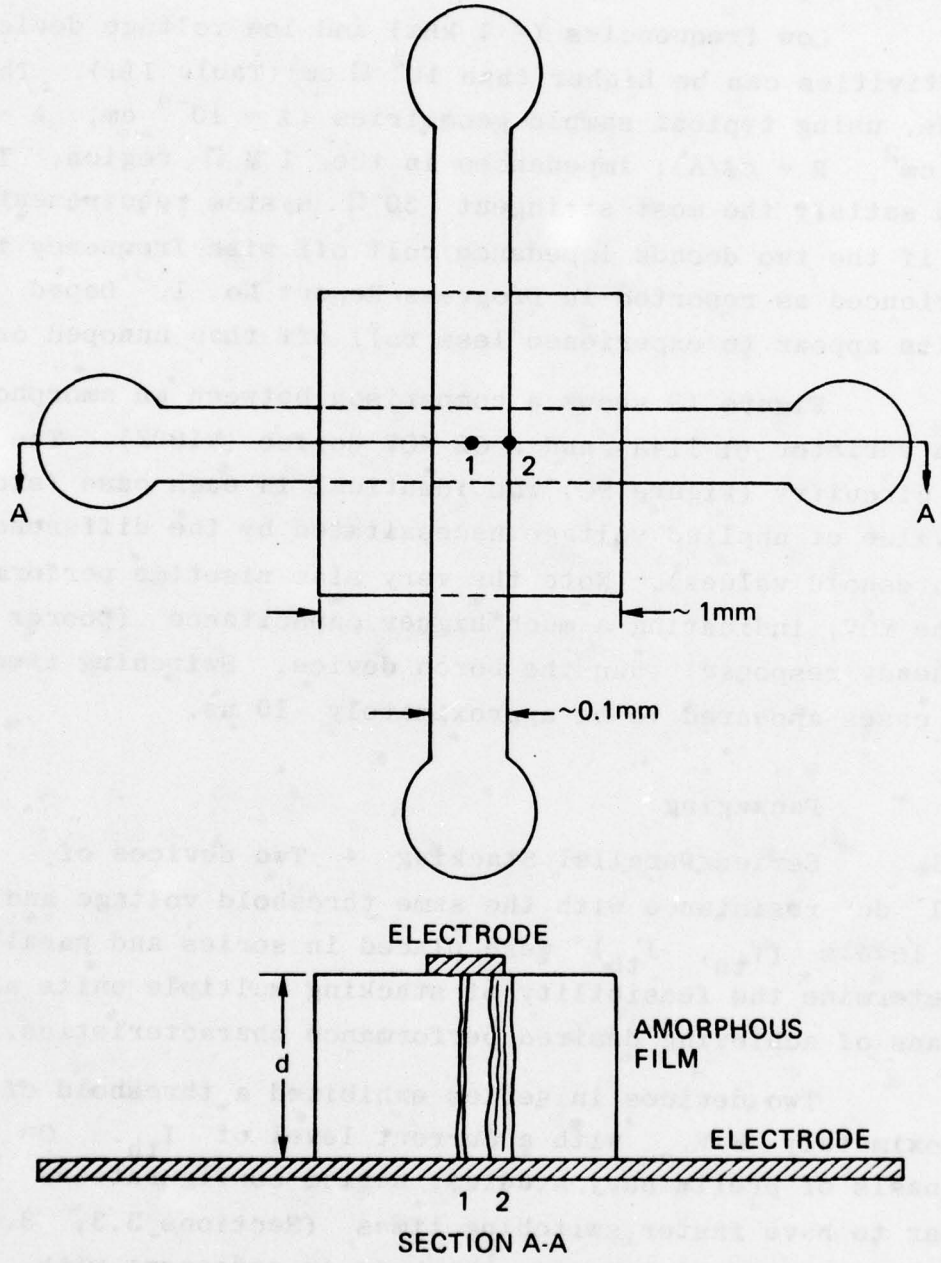


Fig. 12 **Top and Sectional Schematic Views of Amorphous Thin Film Switching Devices. Points 1 and 2 Refer to Locations of the Current Filaments Under Liquid Crystal Observations Film Thickness d Given in Tables III and VI. (drawing not to scale)**

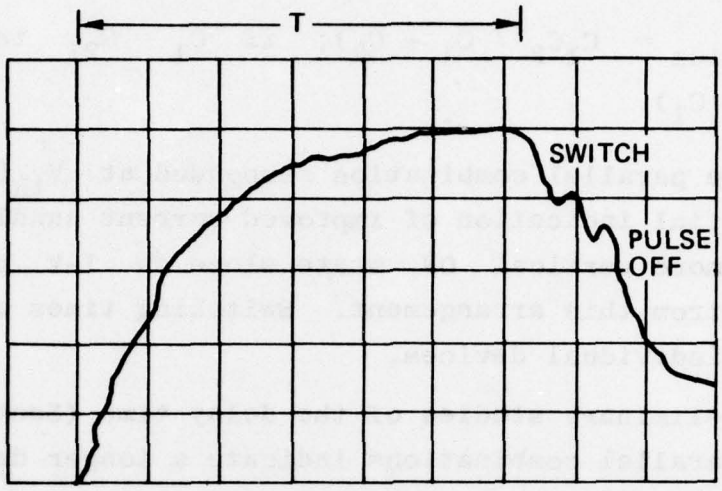
Low frequencies (< 1 kHz) and low voltage device resistivities can be higher than 10^5 Ω cm (Table III). This yields, using typical sample geometries ($\ell = 10^{-4}$ cm, $A = 10^{-4}$ cm^2, $R = \rho\ell/A$), impedances in the 1 M Ω region. This would satisfy the most stringent 50 Ω system requirements even if the two decade impedance roll off with frequency is experienced as reported in Progress Report No. 1. Doped samples appear to experience less roll off than undoped ones.

Figure 13 shows a comparison between an amorphous boron varistor (B 114A) and a GE MOV device (V100Z). The test circuitry (Figure 9C) was identical in each case (except for value of applied voltage necessitated by the differences in threshold values). Note the very slow risetime performance of the MOV, indicating a much higher capacitance (poorer frequency response) than the boron device. Switching time in both cases appeared to be approximately 10 ns.

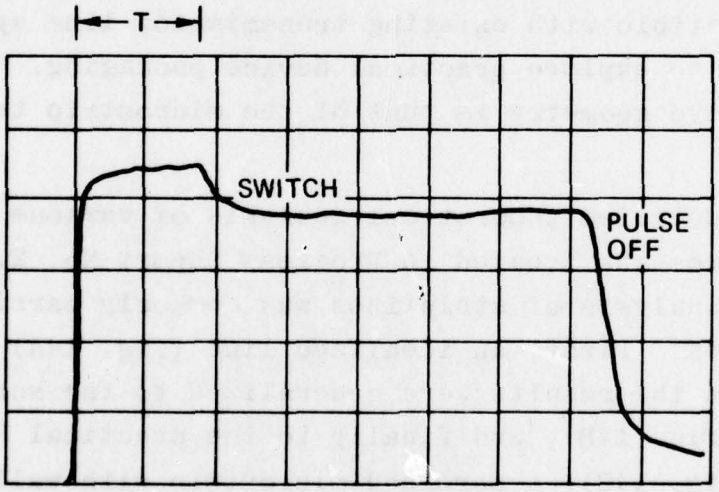
2.9 Packaging

2.9.1 Series/Parallel Stacking - Two devices of equal dc resistance with the same threshold voltage and current levels (V_{th}, I_{th}) were placed in series and parallel to determine the feasibility of stacking multiple units as a means of achieving desired performance characteristics.

Two devices in series exhibited a threshold of approximately 2 V_{th} with a current level of I_{th}. On the basis of preliminary studies, series configurations appear to have faster switching times (Sections 3.3, 3.4) than the individual devices, which is in agreement with recent theories [10,11] based on the switching time being directly proportional to device capacitance



a) GE-MOV V100Z
VERTICAL: 20V/DIV
HORIZONTAL: 10 nsec/DIV
(T = 62.5 nsec)



b) AMORPHOUS BORON: B114A
VERTICAL: 5V/DIV
HORIZONTAL: 10 nsec/DIV
(T = 17.5 nsec)

Fig. 13 Comparison Pulse Switching Characteristic GE-MOV and Amorphous Boron Varistor

(i.e., $C_{series} = C_1C_2 / C_1 + C_2$); if $C_1 = C_2$, then $C_{series} = \frac{1}{2} C_1$).

The parallel combination responded at $V_{th}(2\ I_{th})$ and gave initial indication of improved current handling capabilities (i.e., more vertical ON state slope on I-V plot) as would be expected from this arrangement. Switching times appeared slower than individual devices.

Preliminary studies of the delay time (Section 3.2) for series-parallel combinations indicate a longer delay time for series units while parallel units appear to have the same delay time as individual devices.

2.9.2 Microstrip Analysis - Since final device configurations must be compatible with existing transmission line systems, it is necessary to explore practical device packaging. An especially attractive geometry is that of the microstrip transmission line.

A detailed theoretical analysis of various stripline structures was treated in Progress Report No. 2. The theoretical analysis of striplines was commonly carried out in several stages. First, an idealized line (Fig. 14A) was treated, then the results were generalized to the screened microstrip (Fig. 14B), and finally to the practical "microstrip-in-a-box" (Fig. 14C), a screened microstrip with walls.

The results for the intrinsic impedance of a practical microstrip are summarized by

$W_e/h < 1$ (narrow strips)

$$Z_o\sqrt{2(K+1)} = (376.687/\pi)\left\{\ell n(8h/W_e) + (1/32)(W_e/h)^2 - (1/2)\left[(K-1)/(K+1)\right]\left[\ell n(\pi/2) + (1/K)\ell n(4/\pi)\right]\right\} \text{ ohms} \quad (1)$$

$$W_e/h > 1 \quad \text{(wide strips)} \tag{2}$$

$$Z_o\sqrt{K} = (376.687/\pi)\left[(W_e/2h) + 0.441 + 0.082\left[(K-1)/K^2\right] + \left[(k+1)/2\pi K\right]\left[1.451 + \ell n(W_e/2h + 0.94)\right]\right]^{-1} \text{ ohms}$$

where K is the dielectric constant of the substrate supporting strip, and W_e is an effective width given by

$$W > (h/2\pi) > 2S: \quad W_e = W + (S/\pi)\left[1 + \ell n(2h/S)\right]$$

$$(h/2\pi) > W > 2S: \quad W_e = W + (S/\pi)\left[1 + \ell n(4\pi W/S)\right]$$

A preliminary analysis of the microstrip Equations (1) and (2) indicates that Z_o is essentially independent of S, electrode thickness, if $S \leq 0.1h$ where h is the dielectric thickness. S, however, has to be thick enough to ensure good conductivity (typically a few thousand angstroms). The smallest electrode width is limited by practical manufacturing techniques. Photoetching can produce strips as fine as 2-3 microns but a more practical minimum width is 10 microns. Using Equation (2) and the effective width, W_e, we find for boron ($K_{BORON} = 9.5$) that to have Z_o equal 50 Ω the ratio W/h must be approximately equal to 1($S \leq 0.1h$). This would require a dielectric film thickness of 10 microns.

At present all our films have been less than 3 μm thick (typically 1 - 2 μm) which would yield W/h ratios in the 10 - 5 range, and a Z_o from 10 - 20 Ω respectively. Thicker films appear to be the answer from a strip line point of view. Switching times (Sections 3.4 and 3.5) appear to increase with film thicknesses above 2 μm, indicating support to several authors' [12] claims that switching or varistor mechanisms are thermally induced in thick amorphous films.

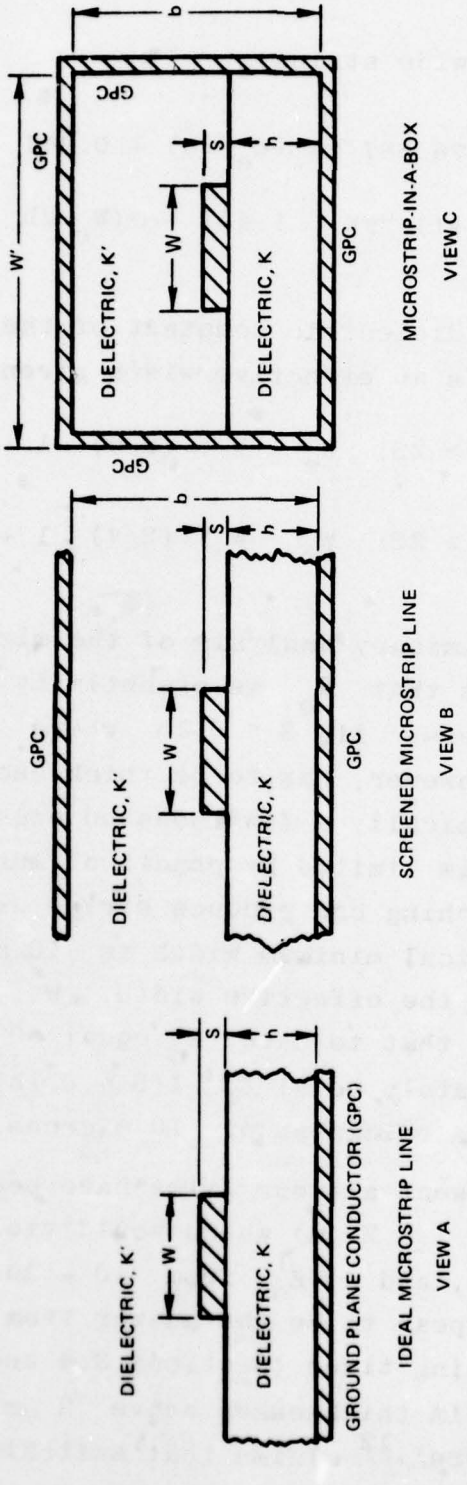


Fig. 14 Cross Sections of Microstrip Transmission Lines

Thus a trade-off has to be made between switching time and impedance. Matching sections will have to be provided in addition to the basic varistor strip line, thus upping insertion loss of device. Short delay time studies at high pulse overvoltages ($T_D \leq 500$ ns) also tend to indicate increases in delay time with increased thickness due to the electronic nature of the switching event (Section 4.2). Narrower electrode widths also could be made by special mask fabrication techniques such as the electron beam method [13].

3. SWITCHING TIMES

To describe the switching times associated with varistor devices, one has to be careful to specify the exact measurement configuration employed. In the following discussion, time descriptions will be referenced to either the curve tracer (Fig. 6a) or pulse measurement systems. Pulse measurements will be distinguished by pulse duration (i.e., $T_D \geq 10$ μs (Fig. 6b) or $T_D \leq 500$ ns (Fig. 9 A, B, C)).

3.1 Description of Times Involved

The times involved in a complete curve tracer cycle are defined with the aid of Fig. 7. The pre-switching portion of this curve has been discussed previously for boron and silicon samples [14,15]. In general, there was always an ohmic region (A-B), followed by a non-linear, Poole-Frenkel or space charge region (B-C), and finally a steeper ($I \sim V^n$) behavior (C-D) where $n > 2$. Proceeding around the switching curve: t_d is the delay time at Point D (determined by pulse techniques); t_1 and t_2 are two switching times observed

during the transition (D-F) to the stable low resistance state (ON state) at Point E. During switching, the initial portion D-E (t_1) always followed the load line, while the portion E-F deviated below (t_2) or above (t_2') the load line. On the return portion of the curve (F-A), there is a reversible region (F-G) and an irreversible spontaneous region (G-B). A recovery time (t_r) is associated with the G-B portion. The switching times were measured at both room and liquid nitrogen temperatures. Sample cooling was achieved by direct immersion in a liquid nitrogen bath.

At room temperature, the D-E portion of Fig. 7 was not always observed and the E-F portion then followed a smooth, non-load line curve (t_2') indicated by the dashed lines. At liquid nitrogen temperature, the distinct times t_1 and t_2 were observed in both silicon and boron samples. The switching times described above (t_1, t_2, t_2', t_r, etc.) were associated with a steady state, i.e., cycled continuously at frequencies less than 1 kHz, with the applied voltage remaining essentially constant during each dynamic transition.

Pulsed I-V characteristics displayed similar features to the forward path (A-F) described in Fig. 7 with the exception that, under single or low repetition rate pulsing, the two mode t_1 - t_2 characteristic disappeared, and a single pulse time, t_p, was associated with the transition from the low to high conductivity state. The usual time constant defined as the 1/e point of the falling voltage versus time characteristic is given by 0.79 t_p.

3.2 Delay Time, t_d

As can be seen from Tables VII and VIII, the time delay ($T_D \simeq 0.1$ ms) appeared to be relatively insensitive to the temperature change from 300 K to 77 K. t_d increased by approximately 15% as the temperature was lowered to 77 K.

In agreement with the observations of others [5], t_d was given by: $t_d = t_{do} \exp(- V/V_o)$ where t_{do} and V_o are empirical constants determined for each sample, and V is the applied voltage ($V_{th} < V < 2V_{th}$). The time delay ($T_D \simeq 0.1$ ms) appeared to possess a statistical nature [5], especially near the threshold where large scatter occurred in the measured values of t_d at a constant overvoltage for the given sample. A detailed discussion of this variation is given by Charles and Feldman [16].

Depending on the samples' threshold, the pulse testing configuration ($T_D \geq 10\ \mu s$) shown in Fig. 6b was limited to applied voltages, V_S, less than $2\ V_{th}$. Above $2\ V_{th}$, the pulsing schemes of Fig. 9 with their inherent short pulse duration (T_D: ~ 80 ns - 500 ns) had to be used. Time delay versus overvoltage ratios for these two measurement schemes are shown in Fig. 15 for applied overvoltages close to V_{th} ($V_{th} < V_S < 2\ V_{th}$). The time delay decreases in a rapid exponential manner. For $V_S > 2\ V_{th}$, the change in time delay with overvoltage is still exponential but the rate of decrease (slope) appears much lower. This indicates that the effect of overvoltage appears to be less in the limit of short duration pulses. Latest measurements have pushed the delay time into the one nanosecond region and the behavior still appears to be exponential. For time delays in the one nanosecond region, it is believed that the breakdown initiation is purely electronic [17]. If this is true, then the pulse threshold voltage (V'_{th}) should exhibit a direct thickness dependence. Experiments to verify this behavior have not yet been conducted.

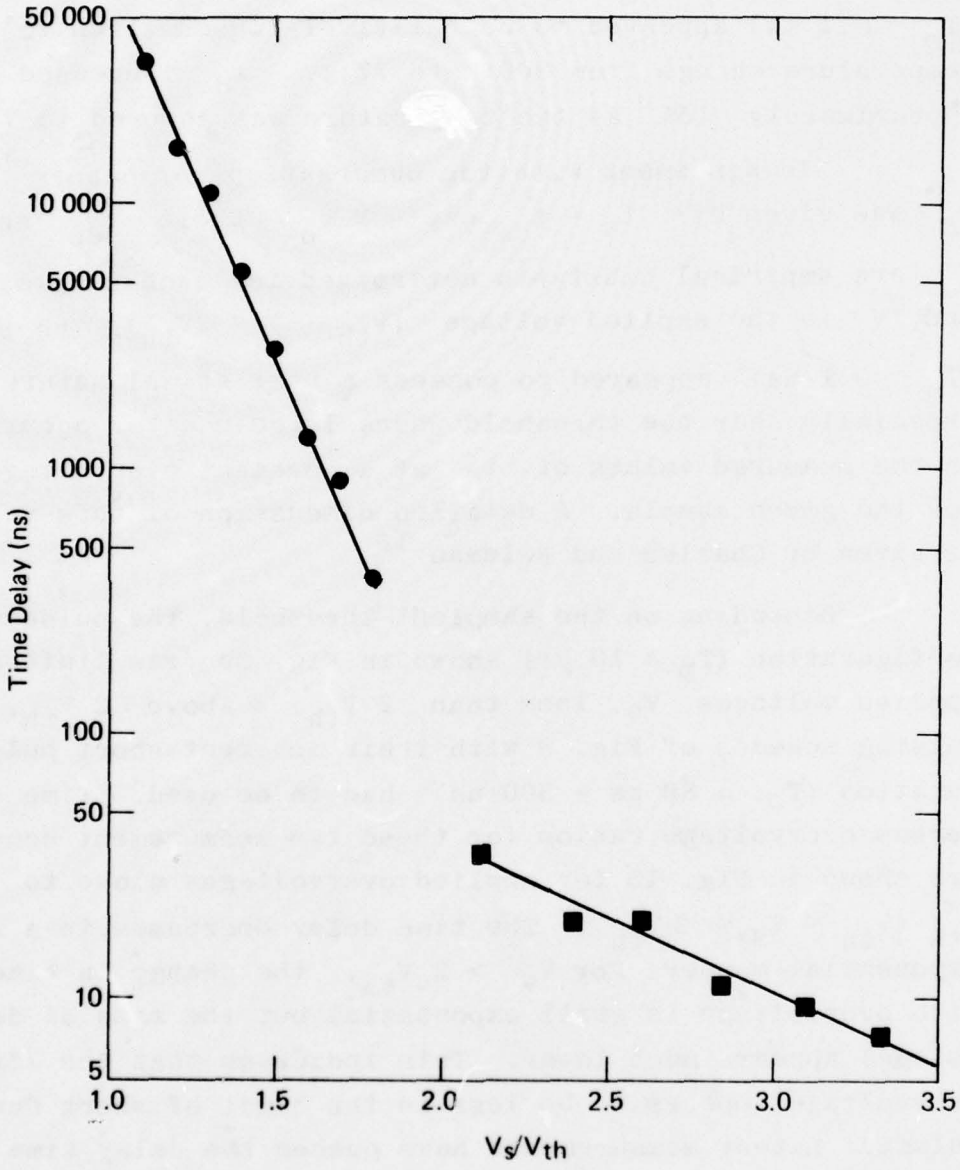


Fig. 15 Time Delay versus Sample Overvoltage Ratio for Amorphous Boron Thin Film at 300K Sample B93A (V_{th} = 10.5 Volts)

● T_D = 0.1 ms (Test Configuration: Figure 6B)
■ T_D ~ 100 ns (Test Configuration: Figure 9C)

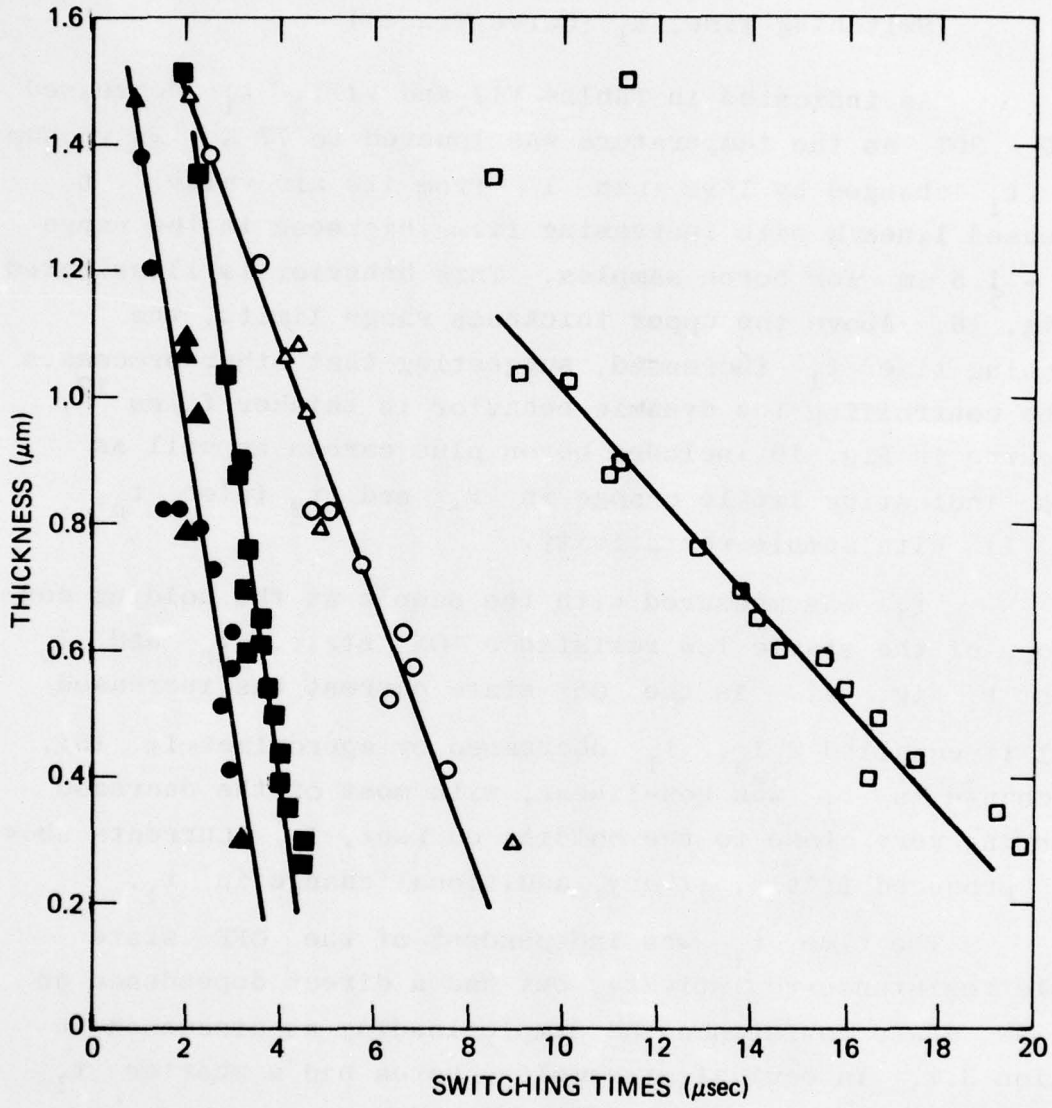


Fig. 16 Switching Times t_1 and t_2 versus Thickness: Amorphous Boron, Boron Plus Carbon, and Silicon Thin Films: 77 K. Boron: ● – t_1 ○ t_2; B+C ▲ - t_1, △ - t_2. Silicon: ■ - t_1, □ - t_2

3.3 Switching Time, t_1 (Curve Tracer)

As indicated in Tables VII and VIII, t_1 decreased by 10 - 30% as the temperature was lowered to 77 K. In vacuum oil, t_1 changed by less than 1% from its air value. t_1 decreased linearly with increasing film thickness in the range 0.15 - 1.5 μm for boron samples. This behavior is illustrated in Fig. 16. Above the upper thickness range limits, the switching time t_1 increased, suggesting that other processes may be controlling the dynamic behavior in thicker films [12]. The curve in Fig. 16 includes boron plus carbon as well as boron, indicating little change in t_1 and t_2 (also t_p, Fig. 7) with sample resistivity.

t_1 was measured with the sample at the holding conditions of the stable *low resistance* ON state, V_h and I_h (Point F, Fig. 7). As the ON state current was increased until it equalled 2 I_h, t_1 decreased by approximately 15%. The change in t_1 was non-linear, with most of the decrease occurring very close to the holding current, I_h. Currents above 2 I_h produced little, if any, additional change in t_1.

The time t_1 was independent of the OFF state sample resistance/resistivity, but had a direct dependence on the ON state resistance and sample loading as discussed in Section 3.7. In equivalent samples, boron had a shorter t_1 than silicon, as can be seen from Fig. 9.

3.4 Switching Time, t_2, (t_2') (Curve Tracer)

The t_2' modes disappeared upon cooling the sample to 77 K, and t_2 modes were decreased in magnitude (30 - 50%). In vacuum oil, both t_2 and t_2' decreased by approximately 2 - 4%.

t_2 for boron decreased linearly with increasing film thickness in the range 0.15 - 1.5 μm, while t_2 for silicon only appeared linear from 0.15 - 1.0 μm (Fig. 16). Above the

1.5 μm thickness limit for boron and the 1.0 μm limit for silicon, the switching time t_2 increased. A thickness dependency of t_2' could not be determined from the data. Although the data displayed wide scatter, t_2 appeared to decrease with increasing OFF state resistance, while t_2' seemed to increase.

The ON state current dependencies of t_2 and t_2' appeared to be similar to t_1, i.e., they decreased by approximately 15% as the steady state ac current (curve tracer) approached 2 I_h. For currents above 2 I_h, they remained essentially constant. Both t_2 and t_2' for silicon samples were longer than t_2 and t_2' of equivalent boron samples (Fig. 16 and Tables VII and VIII).

3.5 Recovery Time, t_r (Curve Tracer)

As can be observed from Tables VII and VIII, the recovery time decreased by 10 - 30% as the temperature was lowered from 300 K to 77 K. In vacuum oil t_r decreased by 2 - 4%.

The dependence of t_r on thickness at room temperature was inconclusive. At 77 K, t_r for pure samples increased linearly with increasing thickness. Boron samples containing carbon displayed a similar trend, but the data possessed considerable scatter.

As the ON state current was increased until it equalled 2 I_h, t_r increased by approximately 15%. t_r continued to increase approximately linearly as the current was raised to 4 I_h.

The recovery time appeared to be independent of the OFF state resistance, but the data displayed some grouping according to impurity content in that t_r (doped) is greater than t_r (undoped). t_r also seemed to be related to the power dissipated just prior to the return switch (Point G, Fig. 7). In general, the more power dissipated, the longer the recovery time.

3.6 Single Pulse Switching Time, t_p

For the circuit in Fig. 6b (T_D > 0.1 ms), the single pulse switching time behaved similarly to t_1. t_p decreased by approximately 15% as the temperature was lowered to 77 K. The inverse thickness dependence of t_p is shown in Fig. 17. As can be seen, t_p started to increase above a thickness of 2 μm. Overvoltage caused t_p to decrease slightly with most of the change (~ 5%) occurring just above threshold. t_p for equivalent samples was less in boron than in silicon.

The single pulse switching time t_p was independent of the OFF state sample resistance. It had a direct dependence on the ON state resistance and sample loading, in fact, time constants derived from t_p compared favorably with the calculated τ_{RC} time constants shown in Tables III and IV.

As the pulse durations decreased, t_p also decreased for a given loading configuration and the agreement with τ_{RC} (determined from circuit path resistance and the measured high voltage capacitance) diminished. Apparently, the pulse duration, time delay, and the device threshold are intimately involved in device capacitance (probably through thermal mechanisms). For short duration pulses (τ_D < 500 ns) using the configuration in Fig. 9C, t_p again compared favorably with an RC time constant, where R is the circuit path resistance and C the geometric or low voltage sample capacitance. t_p's under these conditions are in the 10 ns range. Typical single pulse delay, switching, and response times (t_d and t_p) are given in Table IX. Since the data in Table IX was obtained from a transmission line configuration (Fig. 9C), it is clear that the samples will respond to the proposed EMP signal.

3.7 Switching Time Constant, τ_{RC}

The switching times t_p ($T_D \geq 0.1$ ms), t_1 and t_2, for the same device electrode area were inversely porportional to the sample thickness as illustrated in Figs. 16 and 17. This suggested a relationship between switching and sample capacitance and hence a capacitance discharge behavior as discussed by Klein [10]. The shape of the switching transition does in fact exhibit a reasonable agreement with an exponential discharge characteristic consistent with the relation:

$$V = V_o \exp(-t/\tau_{RC})$$

where $\tau_{RC} = RC$, C = sample capacitance (discussed in Section 2.5), and R = resistance of the discharge path including load, electrode and filament resistance. The filament resistance was assumed to be the difference between the ON state device resistance and the electrode resistance. A curve illustrating the decaying exponential behavior of the switching time t_p ($T_D \simeq 0.1$ ms) for a typical sample (B81D) is shown in Fig. 18. The elapsed time to the 1/e point is 5.5 μs. This compares favorably with the 5.2 μs determined from t_p and the 6.3 μs of τ_{RC}. The generally good agreement between t_p (and its time constant) and τ_{RC} is indicated in Tables III and VII for amorphous boron, and Tables IV and VIII for silicon.

The switching time t_1 was always less than t_p, however the ratio t_1/t_p compares well with the ratio V_{DE}/V_{DF}, where V_{DE} is the ON load line portion of the switching curve (Fig. 7), and V_{DF}, the total voltage drop in the curve. This indicates that the initial portion of the switching transient in the repetitive mode follows a similar behavior as in the single pulse situation ($T_D \geq 0.1$ ms).

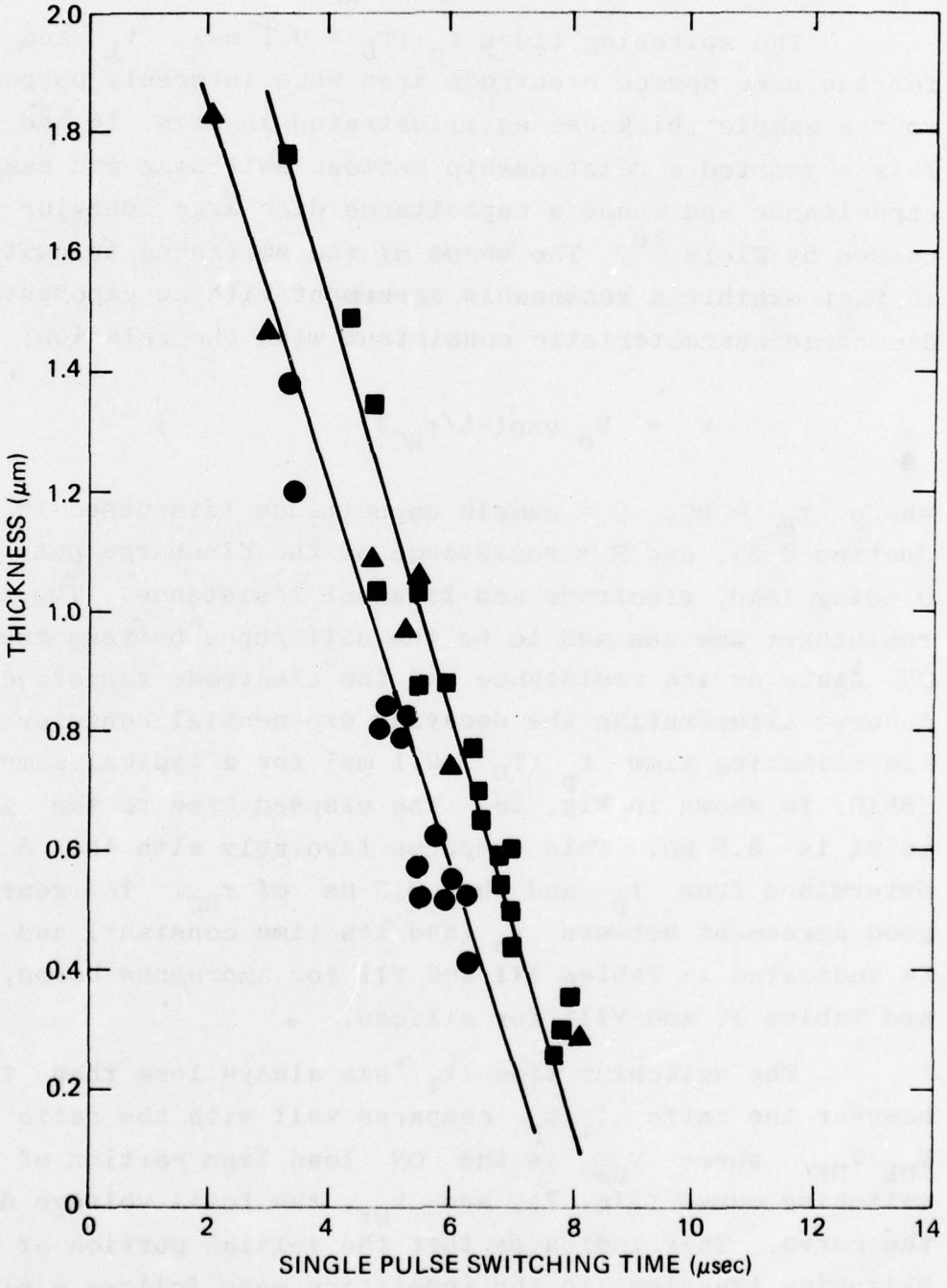


Fig. 17 t_p versus Thickness Amorphous Boron, Boron Plus Carbon, and Silicon Thin Films: 77 K. Boron: ● , B+C ▲ Silicon: ■

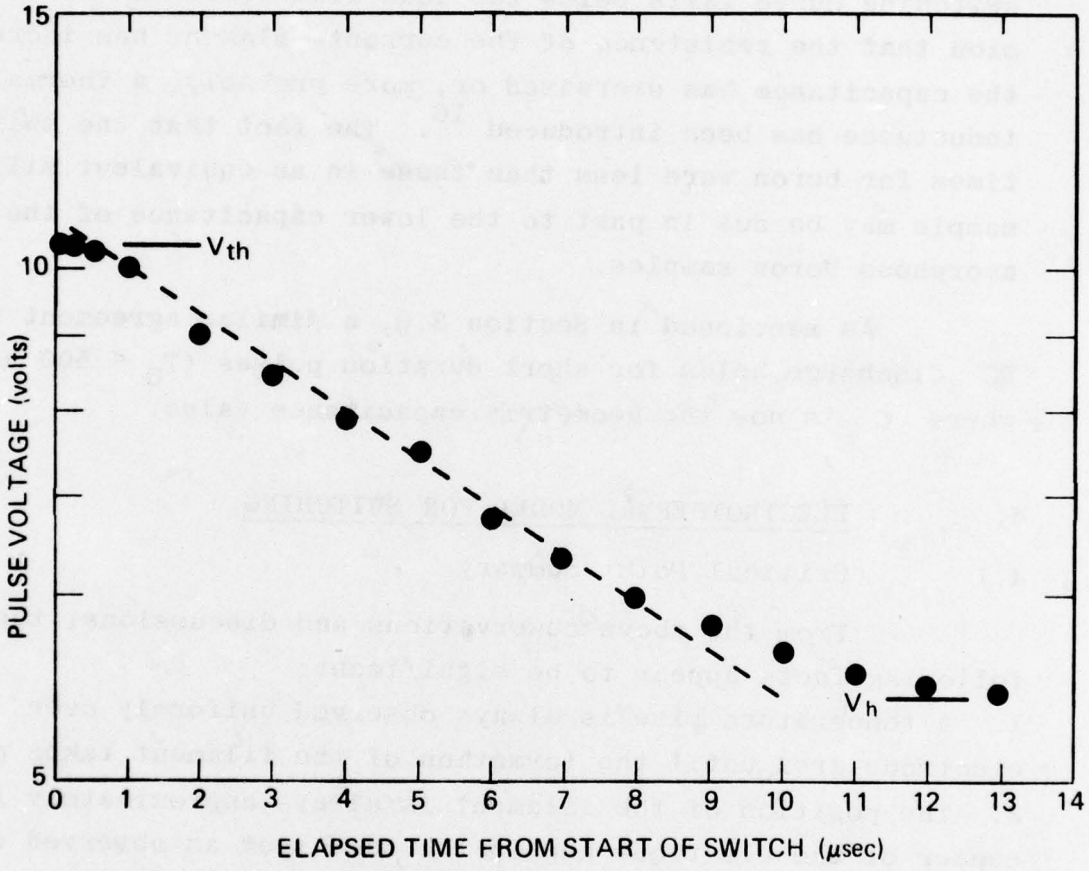


Fig. 18 Pulse Voltage Across Sample versus Elapsed Time from Start of Switch: B81D 77 K.

As can be seen from the slope of Fig. 16, t_2 in both silicon and boron is different from that of t_1, indicating a change in the time constant, i.e., a change in R, C, and/or L. The observation that the current in this portion of the switching curve falls below the load line leads to the conclusion that the resistance of the current filament has increased, the capacitance has decreased or, more probably, a thermal inductance has been introduced [16]. The fact that the switching times for boron were less than those in an equivalent silicon sample may be due in part to the lower capacitance of the amorphous boron samples.

As mentioned in Section 3.6, a similar agreement with RC discharge holds for short duration pulses ($T_D < 500$ ns) where C is now the geometric capacitance value.

4. ELECTROTHERMAL MODEL FOR SWITCHING

4.1 Critical Point Summary

From the above observations and discussions, the following facts appear to be significant:

1. A temperature rise is always observed uniformly over electrode area until the formation of the filament takes place.
2. The position of the filament is always approximately in the center of the electrode and in the same spot as observed cinemicrographically. When current filaments are located on the electrode edges, the switching does not occur along a load line and switching times are longer (t_2').
3. With high repetition rate pulses or at dc, a change in the characteristic occurs during the switching transition, resulting in two separate time constants (t_1 and t_2). In single pulse measurements, only one time constant, t_p, is observed.
4. The delay time (t_d) associated with switching is a strong exponential function of overvoltage. The delay time increases as the sample resistance and/or thickness increases. t_d is slightly longer at low temperatures.

5. Applying a voltage slightly below the threshold and applying heat to the electrodes does not cause the sample to switch; rather the sample becomes more uniformly conducting and tends to become ohmic.

6. Recovery time (t_r) is shorter at lower temperatures and increases with thickness. t_r for silicon is less than for boron. t_r is also longer following the passage of a higher than holding current.

7. The power (P_{th}) at the switching point is lower at liquid nitrogen temperatures than at room temperature.

8. The threshold voltage increases with sample resistance and is approximately $\propto \log R$.

9. Regardless of the shape of the current voltage curve just prior to switching, the curve rises steeply and follows an $I \propto V^n$ dependency.

10. The switching transition, t_p, is inversely proportional to the thickness of the sample and measurements show that the time, τ_{RC}, is about equal to the RC product where C is a sample associated capacitance (Sections 2.6, 3.6 and 3.7), and R is the load and electrode resistance. The shape of the voltage time transition is exponential as expected from the usual capacitance discharge relation.

11. The threshold voltage in the range 0.15 - 1.5 μm is almost independent of the thickness. This is in agreement with earlier measurements on boron films, as well as with measurements on other amorphous semiconductors.

The items 2, 3, 6 and 10 represent new observations. While items 1 through 6 clearly show the existence of thermal processes, items 7 through 11 indicate that more than thermal processes are taking place. Thermal treatments of switching arrive at a $d^{\frac{1}{2}}$ or d dependency of the threshold voltage, V_{th}.

4.2 Postulated Switching Mechanism

To explain these facts, the following steps in the switching mechanism are postulated:

1. Current begins to flow uniformly through the volume of the sample, first by ohmic, and then perhaps by Frenkel-Poole or space charge limited effects (Fig. 19a).

2. This current flow causes a heating of the sample and, because of the geometry, the interior center of the sample becomes hotter than either the edges or the electrode surfaces (Fig. 19b).

3. The hotter portion of the sample has a considerably lower resistance because of the semiconducting nature of the material. Note that the sample is still basically insulator due to the low conduction region near each of the electrodes.

4. The field across the sample now extends from each electrode to the center conducting region, i.e., $E = V_1/d_1$ and V_2/d_2 (Fig. 19c). The distances, d_1 and d_2, are less than the sample thickness and are different, due to influence of the substrate. This field is now extremely high and the sample breaks down through an avalanche or tunnel process.

5. The total charge stored on the sample surfaces (as a capacitor) now flows through this predetermined breakdown path and causes the current conducting filament to form. This filament, once formed, becomes hotter and may change shape by lateral conduction (hence the existence of t_2) (Fig. 19e).

6. The filament is maintained through a thermal process and remains stable until the voltage is lowered. The recovery time depends on the amount of heating that has taken place in the sample.

One can proceed with this model from an almost purely thermal mechanism for switching to an almost purely electronic mechanism, depending on the overvoltage, sample geometry and

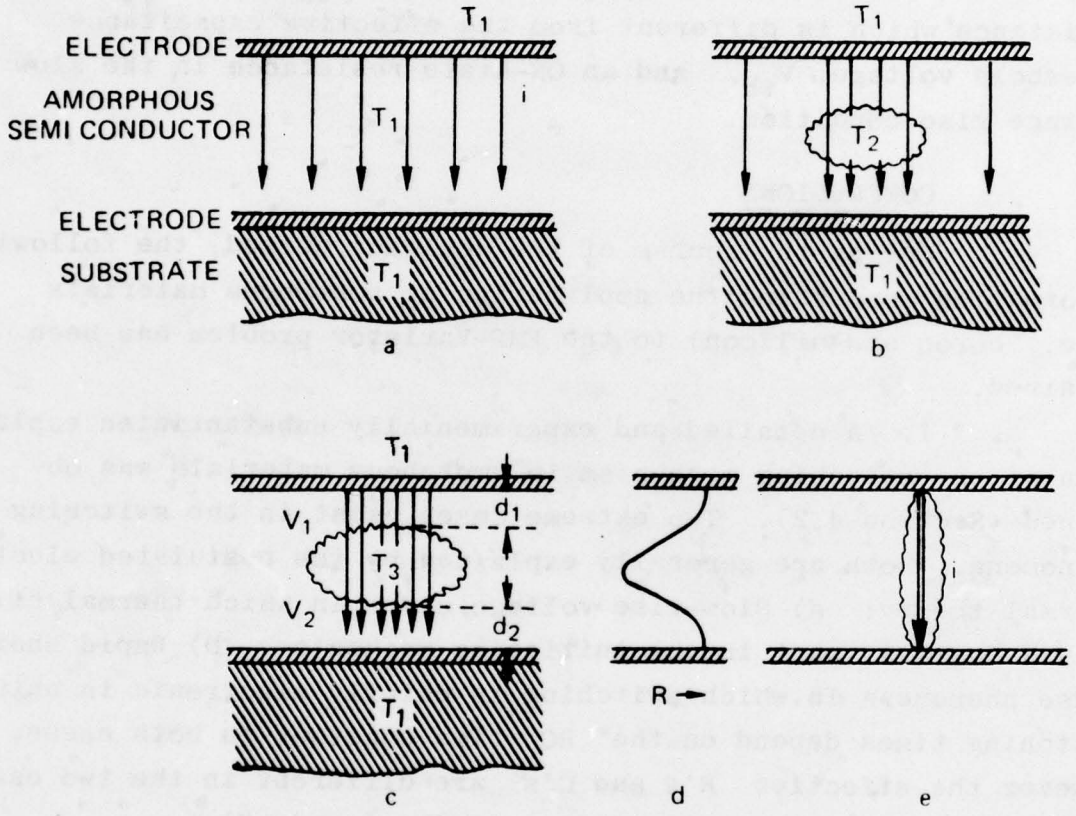


Fig. 19 Postulated Switching Model in Amorphous Semiconductors.
a) Uniform Heating **b) Center Hot Spot**
c) Growth of Hot Spot **d) Resistance Profile**
e) Conducting Filament

pulsing conditions. A very rapid, high voltage pulse will cause chiefly electronic switching because the fields are sufficiently high for breakdown and the sample has not become heated. A slow voltage rise will cause chiefly thermal switching, since the sample has been allowed to heat up until most of the non-conducting portion has disappeared. Associated with the rapid pulse switching is an effective capacitance, a threshold voltage, V'_{th}, and an ON-state resistance which is different from the effective capacitance threshold voltage, V_{th}, and an ON-state resistance in the slow voltage rise condition.

5. CONCLUSIONS

During the course of the contract period, the following information concerning the application of amorphous materials (i.e., boron and silicon) to the EMP-Varistor problem has been obtained.

1. A detailed and experimentally substantiated explanation of the switching mechanism in amorphous materials was obtained (Section 4.2). Two extreme cases exist in the switching phenomena. Both are generally explained by the postulated electrothermal theory: a) Slow-rise voltage cases in which thermal effects play a dominant part in the initiating mechanism. b) Rapid short pulse phenomena in which switching is chiefly electronic in nature. Switching times depend on the RC time constant in both cases, however the effective R's and C's are different in the two cases. Voltage thresholds are also different (V_{th} and V'_{th}).

2. Boron and silicon varistors are symmetric.

3. Boron and silicon thin film varistors, for the given crossover geometry, have capacitances in the 10 pF region, indicating desired frequency behavior above 100 MHz (Section 2.8).

4. Thresholds may be tailored using controlled doping techniques (Sections 2.3 and 2.4). Typical threshold ranges are 5 to 20 volts.

5. The devices may be connected in series and parallel configurations and are compatible with strip line implementation (Section 2.9).

6. Boron varistors may have pulse response times (time delay plus switching times) in the 10 ns range as required by the

nature of the EMP pulse (Sections 2.8, 3.2 and 3.6). With improved device packaging (stripline) it is possible that response times below 1 ns could be achieved.

7. The ON-state resistance was not studied in detail. ON-state resistance varied with pulsing conditions. Generally curve tracer or dc pulse conditions gave a lower resistance than single pulse conditions. The relatively high ON-state resistance (100 Ω), under pulsing conditions, appears to make the devices unsuitable at present for the requirements of a 50 Ω system. It is believed that, with proper choice of materials and dopants in conjunction with parallel device configurations, the ON-state resistance could be reduced.

8. The OFF-state resistance ($\geq 10^3$ Ω) is sufficient to insure no appreciable losses in a normal (non-EMP) 50 Ω system environment.

9. The devices appear to be stable in time and relatively insensitive to environmental effects.

10. The device failure mode appears primarily to originate in the electrodes and not in the amorphous material. This indicates that with improved electrode design an even more rugged varistor could be made.

6. RECOMMENDATIONS

Research has indicated that amorphous varistors may be suitable for use as EMP protection devices. However further research in the following areas is required:

1. The compensatory effect of impurities in amorphous structures.

2. The intrinsic limit of response time and the basic delay mechanisms in sub-nanosecond delays.

3. Understanding the nature of the ON state and the reduction of the ON-state resistance.

4. Power-handling capabilities of given thin film materials and configurations. Failure mode studies.

5. Investigations of worst case environmental and radiation effects and the optimization of packaging configurations.

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TABLE I - Deposition Parameters for Amorphous Boron, Boron Plus Carbon, and Silicon Thin Films

SAMPLE	SUBSTRATE TEMPERATURE °C	DEPOSITION RATE Å/min	DEPOSITION PRESSURE x 10^{-7} Torr	SUBSTRATE MATERIAL	BELL JAR	CRUCIBLE MATERIAL
B55E	120	550	1.7	0211[a]	SS	Ag Plate[b]
B81D	230	825	2.6	Silica	SS	Mo
B68D	300	1140	1.1	Silica	SS	Mo
B88A	200	1040	80.0[c]	Silica	SS	Mo
B98D	300	1240	5.2	Silica	SS	Mo
B67E	250	1460	0.9	Silica	SS	Mo
B83A	500	1370	2.3	Silica	SS	Mo
B86D	700	1200	2.8	Silica	SS	Mo
B86C	700	1230	2.8	Silica	SS	Mo
B91A	300	1590	300.0[c]	Silica	SS	Mo
B92D	500	1350	540.0[c]	Silica	SS	Mo
B93D	300	1290	400.0[c]	Silica	SS	Mo
B94C	700	1060	400.0[c]	Silica	SS	Mo
B97D	300	1260	940.0[c]	Silica	SS	Mo
B89A	300	1330	400.0[c]	Silica	SS	Mo
B95A	300	1220	500.0[c]	Silica	SS	Mo
B96A	300	1430	430.0[c]	Silica	SS	Mo
Si38	240	150	13.0	0211[a]	Pyrex	Cu
Si45	210	380	5.2	0211[a]	Pyrex	Cu
Si35	240	1400	33.0	0211[a]	Pyrex	Carbon
Si42	200	440	13.0	0211[a]	Pyrex	Cu
Si51	240	1000	1.7	0211[a]	Pyrex	Ag Plate[b]
Si57	235	1800	25.0	Silica	SS	Cu
Si48	210	1100	2.0	0211[a]	Pyrex	Ag Plate[b]
Si43	440	300	14.0	0211[a]	Pyrex	Cu
Si50	440	880	3.2	0211[a]	Pyrex	Ag Plate[b]
Si49	440	820	3.3	0211[a]	Pyrex	Ag Plate[b]
Si56	800	625	32.0	Silica	SS	Cu
Si55	800	550	25.0	Silica	SS	Cu
Si54	800	600	38.0	Silica	SS	Ag Plate[b]
Si52	800	760	2.3	Silica	Pyrex	Ag Plate[b]

a) Corning Code Number
b) Silver Plated Copper
c) Partial Pressure C_2H_2

TABLE II

Impurities in Typical Boron Samples as Determined by Sputter-Ion Source Mass Spectrometry

Species	Bulk Boron Atomic Fraction(%)	B98 Atomic Fraction(%)	B93 Atomic Fraction(%)
H	0.44	0.28	0.22
Li	-	0.0008	0.0007
C	0.35	0.33	9.6
N	0.006	0.015	0.0007
O	0.075	0.18	0.084
Na	-	0.0003	0.0006
Mg	-	0.0002	0.0031
Al	0.0028	0.006	0.0015
Si	0.017	0.012	0.012
Cl	-	0.0002	-
K	0.00004	-	0.0004
Ca	0.0007	0.001	0.001
Ti	-	-	0.00004
V	-	0.0014	0.0004
Cr	-	0.001	0.0009
Ba	0.00004	-	-
Cu	-	-	0.0066
Fe	-	0.021	0.0061

TABLE III- Measured and Calculated Parameters for Amorphous Boron and Boron plus Carbon Thin Films

SAMPLE	THICKNESS μm	CARBON ATOMIC %	300 K				77 K		
			ρ_S kΩ.cm	R_S kΩ	C_S nF	τ_{RC} μs	R_S kΩ	C_S nF	τ_{RC} μs
B55E	.29	1.0	1.3	1.9[a]	105.0	9.3	22.0	140.0	8.5
B81D	.41	<0.4	0.9	3.4	60.0	7.2	33.0	55.0	6.3
B68D	.52	0.4	1.5	3.9	52.0	6.7	41.5	47.0	5.9
B88A	.57	1.4	1.0	0.7	42.0	b	15.9	38.0	5.0
B98D	.62	0.4	0.8	0.6	40.0	b	15.2	36.0	5.8
B67E	.73	< 0.4	1.0	3.7	27.0	6.0	39.5	25.0	5.5
B83A[c]	.82	< 0.4	0.8	0.7	28.0	b	19.8	26.0	5.3
B86D[d]	1.20	< 0.4	0.7	1.0	12.0	b	31.0	10.0	3.5
B86C[d]	1.38	< 0.4	0.7	1.1	11.0	b	37.5	10.0	3.6
B91A	.79	6.1	8.3	1.0	23.0	b	46.0	18.0	5.5
B92D[c]	.79	9.6	78.0	10.6	2.5	6.2	89.0	2.1	5.2
B93D	.97	9.8	85.2	14.0	2.8	6.2	115.0	2.5	5.4
B94C[d]	1.06	12.0	39.9	6.8	4.8	6.1	49.6	4.0	5.7
B97D	1.09	15.0	195.0	28.7	1.7	6.0	125.0	1.6	5.0
B89A	1.47	8.2	12.4	3.4	2.5	4.1	43.0	2.2	3.4
B95A	1.83	7.2	10.9	3.3	3.0	3.5	40.0	2.6	2.1
B96A	2.65	3.5	2.5	1.9	6.5	5.6	57.0	5.9	4.8

a) The value of ρ times the measured geometric area did not correlate with R_S for Sample B55.

b) Did not switch at 300 K

c) Deposited at 500°C

d) Deposited at 700°C

TABLE IV - Measured and Calculated Parameters for Amorphous Silicon Thin Films

SAMPLE	THICKNESS μm	300 K				77 K		
		ρ_s kΩ·cm	R_s kΩ	C_s nF	τ_{RC} μs	R_s kΩ	C_s nF	τ_{RC} μs
Si38 [a]	0.27	25.8	3.2	34.0	12.0	60.5	30.0	8.5
Si45	0.50	32.1	5.1	27.0	10.4	85.7	25.0	7.9
Si35	0.70	26.2	7.8	15.0	8.5	97.0	13.0	7.0
Si42	0.88	35.0	8.4	17.5	8.0	100.0	14.5	6.3
Si51	1.03	19.6	3.2	26.0	7.1	61.2	23.0	5.9
Si57	1.50	20.0	4.8	17.5	6.6	81.2	13.5	4.7
Si48	1.77	26.3	8.5	14.0	5.9	102.0	12.0	4.5
Si43 [b]	0.60	30.0	30.0	21.0	9.5	142.5	16.0	7.5
Si50	0.88	33.4	31.6	22.0	7.7	148.0	17.5	6.0
Si49	1.03	22.8	19.0	25.5	6.4	133.0	21.0	5.2
Si56 [c]	0.50	1.9	1.5	29.0	d	55.3	27.0	7.1
Si55	0.55	6.3	4.3	31.0	9.3	70.9	29.0	7.0
Si54	0.60	6.1	4.0	33.0	9.1	65.2	30.5	7.0
Si52	0.77	1.2	1.2	21.0	d	49.5	19.0	6.7

a) Deposited at 200 - 250°C
b) Deposited at 400 - 450°C
c) Deposited at 800 - 850°C
d) Did not switch at 300 K.

TABLE V - Threshold, Holding and Return Voltages and Powers for Amorphous Boron and Boron plus Carbon Thin Films

SAMPLE	300 K						77 K					
	V_{th} Volts	P_{th} mW	V_{th} Volts	P_h mW	V_r Volts	P_r mW	V_{th} Volts	P_{th} mW	V_h Volts	P_h mW	V_r Volts	P_r mW
B55E	4.3	10.4	3.2	22.4	2.6	6.2	4.9	1.37	3.6	15.3	3.3	7.5
B81D	4.2	7.6	3.2	23.7	2.6	6.8	5.1	0.97	3.9	15.6	2.6	6.8
B68D	6.5	10.1	5.3	21.7	4.0	14.0	7.6	1.37	5.4	19.4	5.0	15.7
B88A[a]							5.4	1.94	3.9	20.3	3.2	10.6
B98D[a]							5.2	1.92	3.5	18.6	2.9	10.4
B67E	4.7	11.1	2.8	26.9	2.0	10.0	5.3	1.01	3.0	17.7	2.5	11.6
B83A[a]							5.3	1.05	3.3	16.5	2.9	7.5
B86D[a]							5.6	1.12	3.7	23.3	2.9	14.7
B86C[a]							5.6	1.12	3.5	21.0	2.8	15.0
B91A[a]							7.2	1.30	4.2	30.7	3.3	18.0
B92D	10.4	40.8	5.0	57.5	4.6	34.5	11.1	1.33	5.7	50.7	5.4	38.3
B93D	12.0	36.0	5.6	56.0	5.0	35.0	12.5	1.38	6.2	51.5	5.6	37.5
B94C	9.8	32.3	4.8	44.2	4.1	23.8	10.4	1.14	5.1	31.2	5.2	28.6
B97D	14.2	25.6	9.2	81.9	7.5	52.5	15.0	1.50	10.0	80.0	8.0	54.0
B89A	9.3	32.4	4.5	36.0	4.0	27.2	9.8	1.18	5.2	34.6	4.9	31.6
B95A	9.0	31.5	5.3	50.5	4.5	27.0	9.6	1.25	6.0	40.8	5.0	28.9
B96A	8.5	38.8	5.1	51.0	4.0	18.8	8.9	0.89	6.0	35.5	4.7	21.3

a) Did not switch at 300 K

TABLE VI - Threshold, Holding, and Return Voltages and Powers for Amorphous Silicon Thin Films

SAMPLE	300 K						77 K					
	V_{th} volts	P_{th} mW	V_h volts	P_h mW	V_r Volts	P_r mW	V_{th} volts	P_{th} mW	V_h volts	P_h mW	V_r volts	P_r mW
Si38	5.8	10.7	3.8	12.2	3.5	10.5	6.8	1.05	4.7	10.9	4.5	10.8
Si45	8.0	20.1	5.4	25.1	5.2	18.6	9.8	1.25	6.1	20.3	5.3	19.5
Si35	9.6	24.3	6.0	30.6	5.8	20.5	10.1	1.35	6.9	26.9	5.6	24.2
Si42	10.1	28.0	6.2	31.5	5.7	24.1	11.0	1.40	7.0	30.1	6.3	26.5
Si51	5.7	10.9	4.1	12.9	3.8	9.7	6.4	1.10	5.1	11.8	4.9	10.5
Si57	7.5	18.2	5.4	20.2	5.0	16.5	8.7	1.26	6.5	19.5	6.0	18.7
Si48	10.2	27.7	6.1	43.9	5.2	30.6	11.2	2.70	6.9	38.5	6.1	35.9
Si43	14.6	7.6	8.3	32.5	5.7	18.3	15.4	1.65	8.7	30.6	7.2	23.2
Si50	14.0	7.0	8.0	30.4	5.2	16.6	14.9	1.49	8.4	29.4	6.8	20.4
Si49	15.1	12.1	8.0	40.0	6.0	26.4	16.2	2.43	8.8	38.7	7.7	31.5
Si56[a]							6.5	1.43	3.7	16.7	3.6	10.4
Si55	6.2	11.5	3.9	13.0	3.5	9.5	7.9	1.52	4.5	11.4	4.0	10.8
Si54	5.9	11.1	3.8	12.5	3.4	9.6	7.6	1.47	4.6	11.6	4.1	10.9
Si52[a]							7.5	1.13	6.5	26.0	6.0	22.8

a) Did not switch at 300 K

TABLE VII - Switching Times in Amorphous Boron and Boron Plus Carbon Thin Films

SAMPLE	TIMES, μs 300 K						TIMES, μs 77 K				
	t_d	t_1	t_2	t_2'	t_r	t_p	t_d	t_1	t_2	t_r	t_p
B55E	12.5			89.7	39.7	9.0[a]	18.0	3.1	9.1	27.2	8.1
B81D	8.9			55.0	30.9	7.0[a]	12.5	2.9	7.6	20.3	6.5
B68D	9.8	2.8	11.4		43.6	6.0	13.0	2.5	6.8	28.7	5.5
B88A[b]							9.8	3.0	6.7	24.2	5.4
B98D[b]							9.4	2.9	6.5	24.5	5.8
B67E	10.7			70.3	39.2	5.6[a]	13.5	2.6	6.0	28.0	5.4
B83A[b]							9.5	2.0	4.9	20.5	5.0
B86D[b]							11.8	1.1	3.7	28.6	3.4
B86C[b]							12.0	1.0	2.5	29.8	3.3
B91A[b]							23.0	2.3	5.6	34.1	5.0
B92D	35.0	3.0	10.0		62.5	5.6	38.0	2.5	5.5	51.3	4.8
B93D	33.0	2.5	7.3		63.7	5.9	35.5	2.3	4.4	50.9	5.3
B94C	27.1			100.0	52.7	5.7[a]	31.0	2.0	4.2	46.3	5.5
B97D	40.3	2.1	6.5		84.8	5.3	49.3	2.0	4.5	78.6	4.7
B89A	20.5	1.2	4.2		54.3	3.5	27.5	.9	2.0	47.2	3.0
B95A	20.1			130.0	56.6	2.5[a]	25.0	.8	3.0	45.7	2.0
B96A	15.0			250.0	46.1	6.1[a]	19.0	2.6	7.6	35.8	5.0

a) Under pulse testing, t_2' modes frequently did not occur. Times listed are average of t_p's when t_2' was absent.

b) Did not switch at 300 K

TABLE VIII Switching Times in Amorphous Silicon Thin Films

SAMPLES	300 K: TIMES, μs						77 K: TIMES, μs				
	t_d	t_1	t_2	t_2'	t_r	t_p	t_d	t_1	t_2	t_r	t_p
Si38	48.4	5.2	26.5		22.7	11.4	50.1	4.5	19.8	14.5	7.3
Si45	45.1			127.3	33.6	9.5[a]	48.3	4.0	16.3	24.2	7.0
Si35	40.6	4.0	20.1		40.7	7.9	44.9	3.3	13.8	32.5	6.5
Si42	39.2	3.9	18.3		43.9	7.3	41.7	3.1	11.2	34.8	5.9
Si51	37.1	3.5	17.5		23.0	6.6	40.0	2.8	10.1	14.0	5.4
Si57	31.7	3.0	19.0		31.2	6.1	35.6	2.2	11.6	23.6	4.4
Si48	30.8			163.1	50.1	6.0[a]	33.9	2.1	12.3	45.0	4.3
Si43	46.1	4.6	24.3		40.1	8.7	53.2	3.6	15.5	30.5	6.9
Si50	44.0	4.1	20.1		35.0	7.4	50.6	3.0	11.0	23.6	5.5
Si49	40.5	3.6	16.4		45.9	6.1	44.0	2.7	9.1	40.2	4.8
Si56[b]							20.1	4.0	16.8	17.0	7.0
Si55	18.3	4.8	25.1		20.5	8.9	20.5	3.9	15.9	14.7	6.8
Si54	18.0	4.6	24.8		21.4	8.5	19.8	3.5	15.5	14.9	6.7
Si52[b]							22.5	3.3	12.9	28.5	6.4

a) Under pulse testing, t_2' modes frequently did not occur. Times listed are average of t_p's when t_2' was absent.

b) Did not switch at 300 K.

TABLE IX

Typical Short Duration Single Pulse Response Parameters

SAMPLE NO.	THICKNESS μm	V_{th} VOLTS	V'_{th} * VOLTS	T_D ns	t_d ns	t_p ns	(t_d+t_p) ns
B93F	0.85	9.8	24.5	66.4	18.9	3.4	22.3
B114A	1.20	10.3	28.3	65.6	21.9	6.0	27.9
B136D	0.85	9.8	22.2	69.6	12.6	7.5	20.0
B141A	1.25	9.5	51.0	70.0	10.0	11.0	21.0
B143D	1.50	8.0	38.0	66.0	20.0	9.0	29.0
B134D	0.28	2.75	22.7	77.3	6.7	3.0	9.7
B135A	0.80	3.25	36.6	79.2	34.2	8.1	42.3

* V'_{th} represents the threshold voltage at pulse duration T_D.

LIST OF SYMBOLS

A	Cross Sectional Area	t	Time
C	Effective Capacitance	t_1	Initial Switching Time
C_s	Threshold Capacitance	t_2, t_2'	Final Switching Time
d	Thickness	t_d	Delay Time
d_1, d_2	Effective Thickness	t_{do}	Constant
E	Electric Field	t_p	Pulse Switching Time
f	Frequency	t_r	Recovery Time
h	Dielectric Thickness	τ_{RC}	Time Constant
I	Current	$T_{1,2,3}$	Temperature
I_h	Holding Current	T_D	Pulse Duration
I_r	Recovery Current	T_R	Risetime
I_{th}	Threshold Current	V	Voltage
K, K'	Dielectric Constant	V_o	Constant
K_o	Constant	V_h	Holding Voltage
ℓ	Thickness	V_p	Pulse Voltage
n	Constant	V_r	Recovery Voltage
P_h	Holding Power	V_s	Sample Voltage
P_r	Recovery Power	V_{th}	Threshold Voltage
P_{th}	Threshold Power	V_{th}'	Pulse Threshold Voltage
R	Effective Resistance	W	Microstrip Width
R_s	Low Voltage Resistance	W_e	Effective Microstrip Width
ρ	Resistivity	Z	Impedance
ρ_s	Sample Resistivity	Z_o	Characteristic Impedance
S	Microstrip Thickness		